

# Investigation of 4T CMOS Image Sensor Design and the Effects of Radiation Damage (MPhys Dissertation)

Adam Godbeer

*Department of Physics, University of Surrey, Guildford, Surrey, GU2 7XH, United Kingdom*  
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## ABSTRACT

Three test structures of the first 4T image sensor design created at the Rutherford Appleton Laboratory, FORTIS 1.0, were optimised and characterised. Each test structure differed in their active area shape, source follower size and core pixel design. Three different processing variations were also tested. The differences between the processing variations proved minimal but the results for each test structure varied significantly, with the best test structure producing a quantum efficiency of  $(31.0 \pm 0.2) \%$  and conversion gain of  $(2.47 \pm 0.02) \text{ DN/e}^-$ . It also boasted the lowest average noise results for a RAL CMOS sensor at  $(6.0 \pm 0.5) \text{ e}^-$ , reaching as low as  $5.7 \text{ e}^-$ . The radiation hardness of FORTIS 1.0 is also investigated with its best pixel structure being exposed to varying amounts of ionising radiation (50kV X-rays). It is shown to be tolerant (and able to fully recover from) a radiation exposure of at least 2.2 kGy.

An updated revision of the design, FORTIS 1.1, was also compared to its earlier counterpart. The effects of a specialised low-noise process used in the manufacture of this revision are confirmed to be positive after a direct comparison with the untreated FORTIS 1.0. Finally, the creation of analysis software used for this project is discussed and future radiation hardness tests for FORTIS 1.1 are outlined.

## **ACKNOWLEDGEMENTS**

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## **ABBREVIATIONS**

RAL = Rutherford Appleton Laboratory

MOS = metal–oxide–semiconductor

MOSFET = field-effect transistor

CMOS = complementary metal–oxide–semiconductor

NMOS = N-type (negative-type) metal–oxide–semiconductor

PMOS = P-type (positive-type) metal–oxide–semiconductor

DSNU = dark signal non-uniformity

PRNU = photon response non-uniformity

FORTIS = 4T test image sensor

Rad hard = radiation hardness

QE = quantum efficiency

RTS noise = random telegraph signal noise

ADC = analogue-digital converter

ESA = European Space Agency

GUI = graphical user interface

RAM = random access memory

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## **(1) INTRODUCTION**

When considering image sensors, there are two major competing designs – CCDs (Charged Coupled Devices) and CMOS (Complementary Metal–Oxide–Semiconductor) image sensors. CCDs are a type of passive image sensor, meaning that the charge collected by a pixel is transported across the chip (often to a single corner of the array), converted to a voltage and outputted as an analogue signal to be digitised off-chip. CMOS image sensors are a type of active pixel sensor; each pixel has its own charge-to-voltage conversion circuitry and often additional circuitry for voltage amplification and on-chip analogue-to-digital conversion.

Today, both types of image sensor are common in both professional and consumer grade products. Neither technology has a clear overall advantage over the other but both have their own benefits that lend themselves to different applications. The strengths of CCDs are typically low noise, high light sensitivity and generally high quality images. CMOS image sensors are superior in their ability to incorporate extra processing functions within the pixel circuitry, their lower power usage (due to the typically lower voltages used), reduced image lag and the ability to read single pixels individually. CMOS designs are also cheaper to produce but CCDs have been mass produced for a longer period of time, so the technology is more mature.

Many technological breakthroughs have hinted at the possibility of one sensor type becoming the de-facto standard for most applications because one of its weaknesses has been suppressed but so far, neither has found overall dominance. Currently, CCDs and CMOS image sensors are complementary technologies, each with their own applications, and it looks to remain that way

for the next decade at least. For example, the superior image quality of CCDs lends themselves to professional cameras, whereas the low power consumption of CMOS image sensors has secured their use in the camera phone market.

The CMOS Sensor Design Group, part of the Technology Business Unit at the Rutherford Appleton Laboratory, designs CMOS image sensors for many different scientific applications, such as X-Ray medical physics, particle physics and space science. The group currently consists of 7 permanent employees as well as one or two placement students each year.

### **(1.1) PHYSICS OF IMAGE SENSORS**

The primary mechanism behind light detection in image sensors is electron generation by incoming photons. This process is called *photogeneration* and is explained below.

Electrons in all solids can only have energies within certain bands, which correspond to a number of discrete quantum states. Most states close to the nucleus are typically full and electrons in these states are closely bound to the atom – these states comprise the *valence band*, defined as the highest band of electron energies that are full when at a temperature of 0K. Beyond this band is the *conduction band*, where electrons are not as closely bound to the atom and are free to accelerate under the influence of an applied electric field and thus form part of an electric current. In metals, there is no energy gap between these two bands, which is why they can conduct electricity with ease. In insulators, there is a large energy gap between the two bands, known as a *band gap*. Semiconductors are special in that they have a band gap

but it is relatively small, so less energy is required to excite an electron into the conduction band.

In order to excite an electron from the valence band into the conduction band (*generation*), it must receive energy, typically from either heat or a photon. For an incident photon to “free” an electron, it must have energy greater or equal to that of the band gap of the material. When an electron moves into the conduction band, it leaves behind what is called a *hole*, the conceptual absence of electron, in the valence band. At finite temperatures, random vibrations due to thermal energy will cause hole-electron pairs to form and disappear (*recombination*) throughout a semiconductor. When the generation and recombination rates are equal, a stable background concentration of electrons and holes is created.

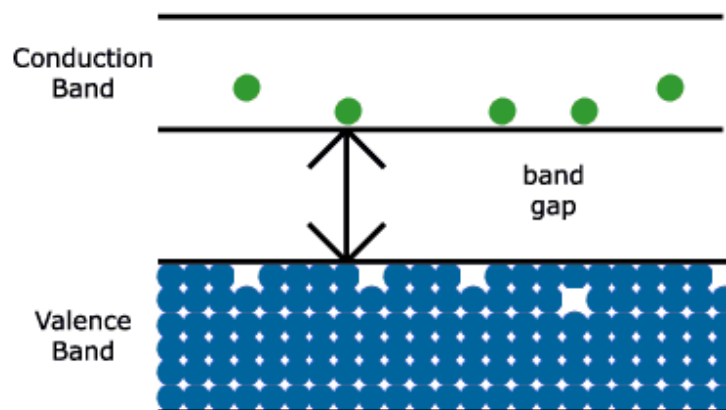


Fig. 1 – Band gap in semiconductors <sup>[2]</sup>

Because incoming photons can only free an electron if their energy equals or exceeds that of the band gap, and the energy of a photon is denoted by its frequency, there is a minimum frequency (and thus maximum wavelength) of photons that can be detected:

1

$$E = hf = \frac{hc}{\lambda}$$

2

$$E_g = \frac{hc}{\lambda_m} \quad \text{(where } E_g \text{ is the band gap energy, } \lambda_m \text{ is the maximum detectable wavelength)}$$

Silicon, the most commonly used semiconductor in solid state electronics, has a band gap of 1.12eV at 300K, corresponding to  $\lambda_m$  equal to 1.11 $\mu$ m. This wavelength belongs to the infrared portion of the electromagnetic spectrum. It is interesting to note that, because of this, most cameras can detect infrared and require a filter in the lens to remove this information from normal images. The absorption of incident photons is not linear with photon energy (and therefore neither wavelength), however, and is defined by the absorption coefficient. The energy absorbed at a certain depth  $x$  is given by:

3

$$E_x = E_0 \cdot e^{-ax} \quad \text{(where } E_0 \text{ is the energy reaching the surface of the semiconductor, } x \text{ is the depth and } a \text{ is the absorption coefficient)}$$

The absorption coefficient is a strongly decreasing function of wavelength (as shown in *Fig. 2* below). Typical absorption depths ( $\alpha^{-1}$ , defined as the distance at which the intensity of light is reduced to  $e^{-1}$ , or ~36%, of its original intensity) for silicon vary between 100 $\mu$ m for infrared and 10nm for ultraviolet photons.



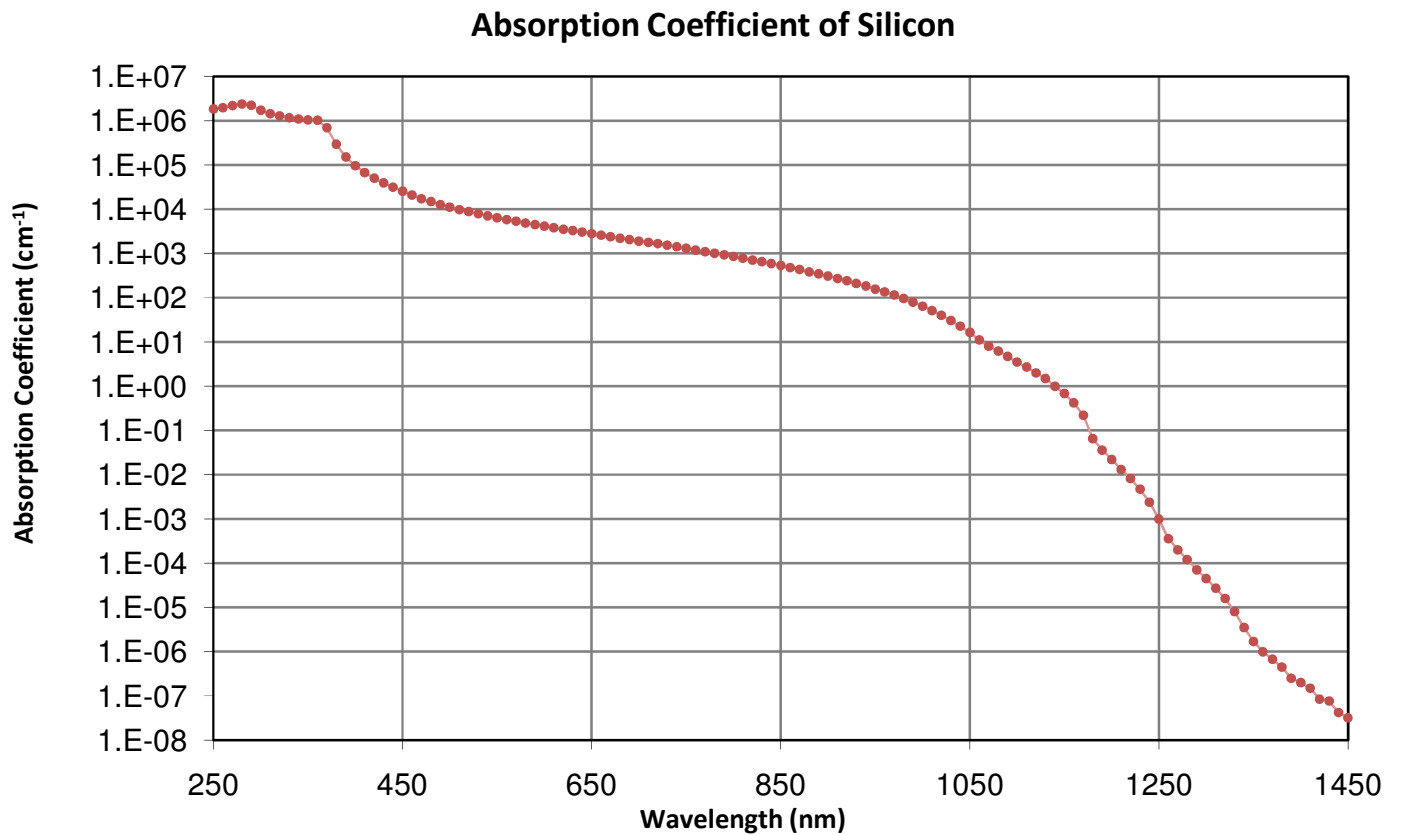
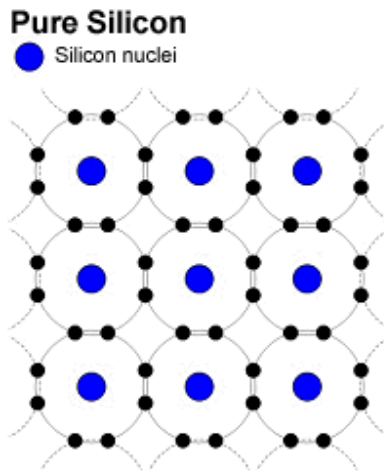


Fig. 2 – Absorption coefficient of Silicon as a function of wavelength <sup>[4]</sup>

#### (1.1a) Doping

In its purest form, silicon (a group 14 element) has four valence electrons. In order to change its electrical properties, the silicon can be subject to a process called *doping*. This involves introducing impurities from group 13 or 15 (which have three or five valence electrons, respectively) in order to increase the number of electrons or holes. This can be done using either *diffusion* or *implantation*.



*Fig. 3 – Silicon lattice valence bonds* <sup>[3]</sup>

### **(1.1b) N-Type Semiconductors**

The *N* here stands for *negative*. In the case of silicon, this type of semiconductor is produced by adding an impurity of group 15 elements into the lattice. An example of a dopant used in this way is phosphorus. These *donor atoms* have five valence electrons, so when inserted into the lattice, will have four covalent bonds and an unbounded electron. Because this free electron is only weakly bound to the atom, it can be easily excited into the conduction band. Because it was not previously in the valence band, no hole is left, thus the number of electrons exceeds that of the number of holes. However, it should be noted that the overall charge of an N-Semiconductor is zero because whilst there are more electrons, there are also immobile dopant ions.

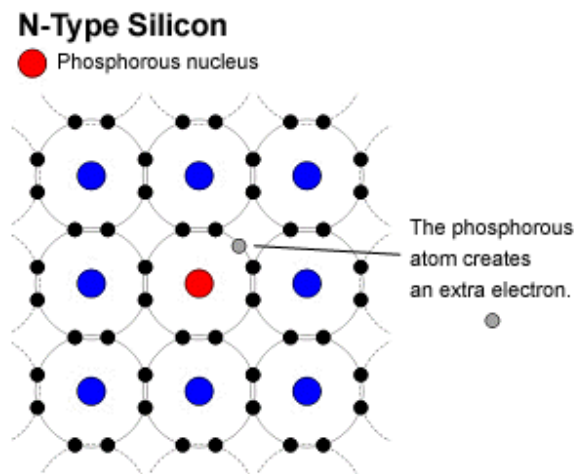
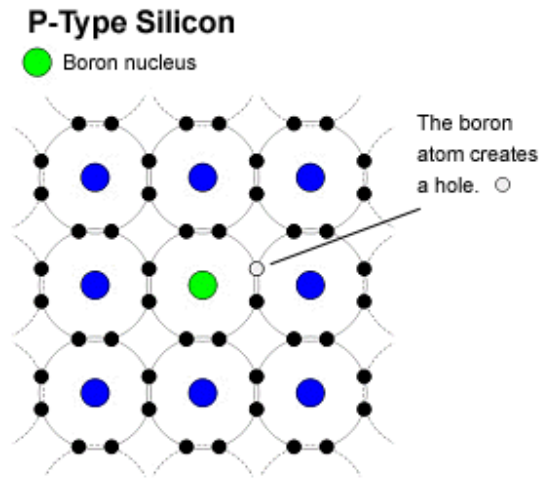


Fig. 4 – Silicon lattice doped with Phosphorous atoms <sup>[3]</sup>

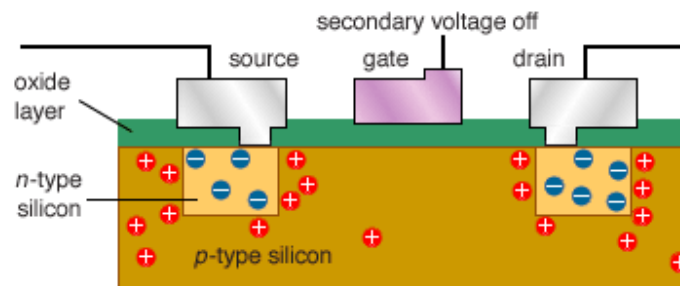
### (1.1c) P-Type Semiconductors

The *P* here stands for *positive*. In the case of silicon, this type of semiconductor is produced by adding an impurity of group 13 elements into the lattice. Examples of dopants used in this way include boron and aluminium. These *donor atoms* have three valence electrons, so when inserted into the lattice, will have a missing electron from one of the four covalent bonds that is normal for a silicon lattice. This can be remedied by accepting an electron from a neighbouring atom, which results in the formation of a hole. Again, the net charge of the sample is typically zero because each hole is associated with a negatively-charged ion. However, once the hole has separated from its ion, one proton in this atom containing the hole is no longer cancelled by an electron. Because of this, the hole acts as a positive charge and the number of holes exceeds the number of excited electrons.



*Fig. 5 – Silicon lattice doped with Boron atoms*<sup>[3]</sup>

These p-type and n-type semiconductors can be used to create what are known as PMOS and NMOS field-effect transistors (MOSFETs). MOSFETs are essentially voltage controlled switches and are the building blocks of CMOS circuits. The operation of an NMOSFET is explained below; PMOSFETs are also used in CMOS circuitry and operate in similar manner.



*Fig. 6 – NMOSFET, an NMOS field-effect transistor*<sup>[5]</sup>

In an NMOSFET (see Fig. 6), a p-type semiconductor is the main substrate used, with a small amount of n-type semiconductor material connected to the source and drain paths. When there is no voltage applied at the *gate* ( $V_G = 0$ ), no flow between the source and drain occurs ( $V_{GD} = 0$ ). When a small positive (in the case of an NMOSFET) voltage is applied at the gate, the holes in the p-type substrate are repelled and a *depletion region* forms between the insulating (oxide) layer and the substrate (which is the p-type silicon in this example). By itself, this does not affect

the lack of current between the source and drain. However, if the gate voltage exceeds a certain level, an inversion layer between the insulating (oxide) layer and the substrate (which is the p-type silicon in this example) forms in the depletion region. An *inversion layer* is simply a layer with opposite charge to that of the rest of the substrate – in this case, a layer of electrons that is oppositely charged to the holes in the p-type silicon. With the inversion layer in place, a current can flow across it when a voltage is applied between the source and drain, as shown in Fig. 7.

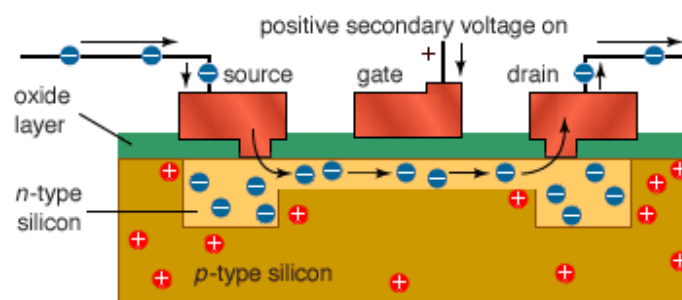


Fig. 7 – NMOSFET, with a positive gate voltage applied <sup>[5]</sup>

The voltage required for the creation of this inversion layer is called the *threshold voltage*. When the gate voltage exceeds that of the threshold voltage ( $V_{GS} > V_{Th}$ ), the inversion layer that appears allows for the flow of current between the source and drain ( $I_{DS}$ ).  $I_{DS}$  can be increased by raising  $V_{GS}$  or  $V_{DS}$  but only up to the point where  $V_{DS} = V_{GS} - V_{Th}$  (called the *pinch off point*), where varying  $V_{DS}$  no longer affects  $I_{DS}$ . In this situation, where only  $V_{GS}$  continues to affect  $I_{DS}$ , the MOSFET is said to be operating in *saturation* mode. Current still flows between the source and drain but, because the inversion layer no longer provides a direct channel between them, this is due to the electric field generated by the voltage between the source and drain.

## (1.2) PHOTODIODES

Photodiodes are the most common type of light detectors used in CMOS image sensors. They are usually made up of a PN junction (a p-type and n-type semiconductor joined together,

typically by implanting n type dopants into p-type silicon or vice-versa), where the free charges in both semiconductors diffuse towards each other due to concentration differences. When equilibrium is achieved, this results in the formation of a *charge-free* region, also known as the depletion region (see Fig. 8). The remaining charges on each side feel an electric field which counters the *diffusion force* that is attracting them to the charge-free region so they remain where they are, resulting in three regions in the PN junction: the *p-neutral region*, the *n-neutral region* and the *charge-free region*. In equilibrium, ideally no charge flows. In reality, there is a small leakage or *dark current*, caused mainly by imperfections in the silicon.

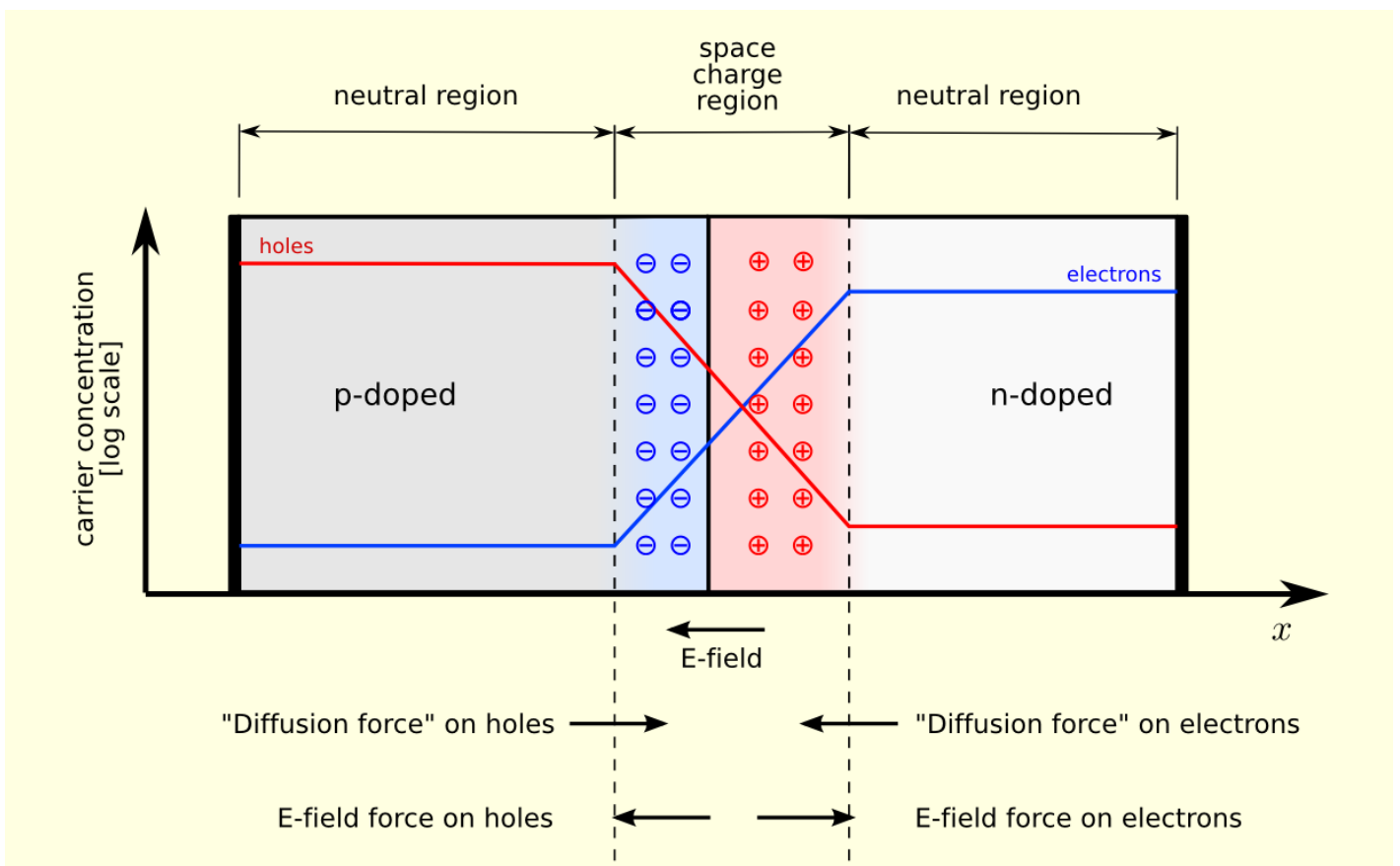


Fig. 8 – PN junction in equilibrium<sup>[14]</sup>

PN junctions can be connected to an external voltage to create either *forward* or *reverse bias*. Reverse bias, whereby the negative terminal of the battery is connected to the p-type semiconductor and the positive terminal is connected to the n-type semiconductor, is used for photodiodes. Reverse bias causes the depletion region to expand, increasing the junction's capacitance. This, along with the larger field strength in the depleted region, causes carriers to move more quickly, thus improving response times. Another advantage of using reverse bias is that it allows the storage of the photocurrent, something which is not possible when using forward bias.

The basic operation of a PN junction when used in a photodiode involves photons entering the depletion region, exciting free electrons and holes, which then migrate to the n-type and p-type regions, respectively, producing a detectable current.

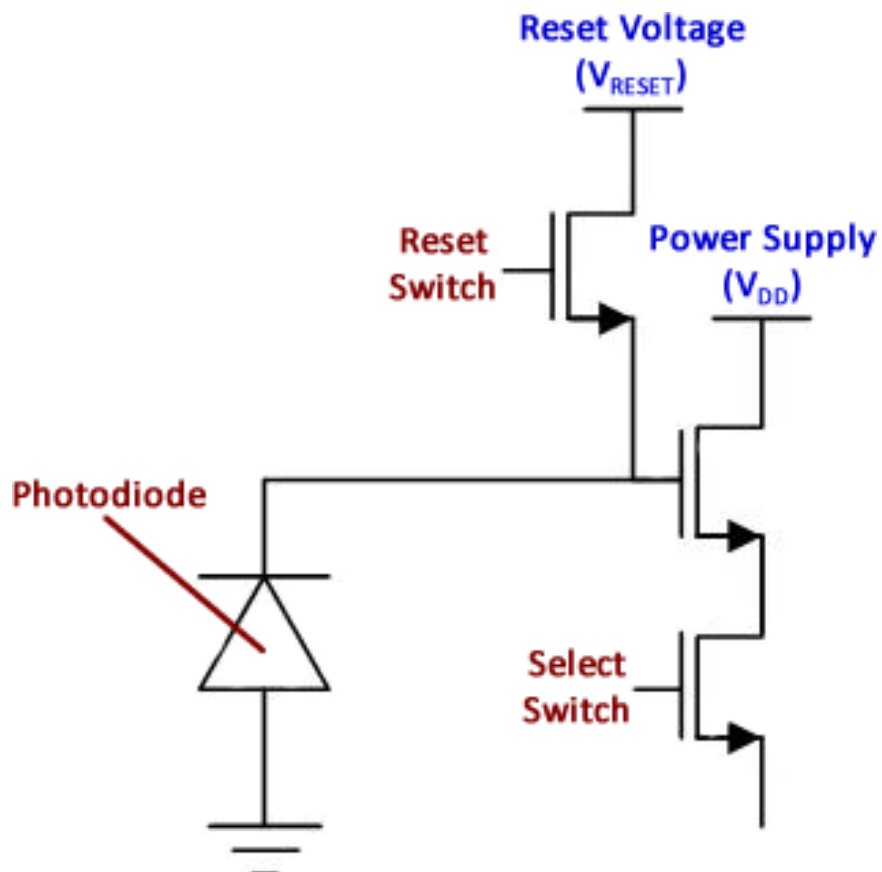
Another important benefit of reverse bias is that it causes the depletion region to expand. This is a useful trait for photodiodes because the absorption coefficient varies with wavelength (see *Equation 3* and *Fig. 2*), meaning the depletion region should be as large as possible in order to provide a good spectral response. For most sensors, the best response is for green light (~546nm) as it is absorbed mostly in the depletion region.

## (2) THEORY

### (2.1) CMOS Image Sensors

An image sensor is a 2D array of photo-sensitive pixels that, when the data from them is correctly acquired and processed, produces an image. The simplest type of pixel contains a single transistor but the most common type of pixel in scientific applications currently is the traditional 3T image sensor. 3T pixels contain three transistors (hence their name), as shown in

*Fig. 9:*



*Fig. 9 – 3T Pixel (adapted from<sup>[15]</sup>)*



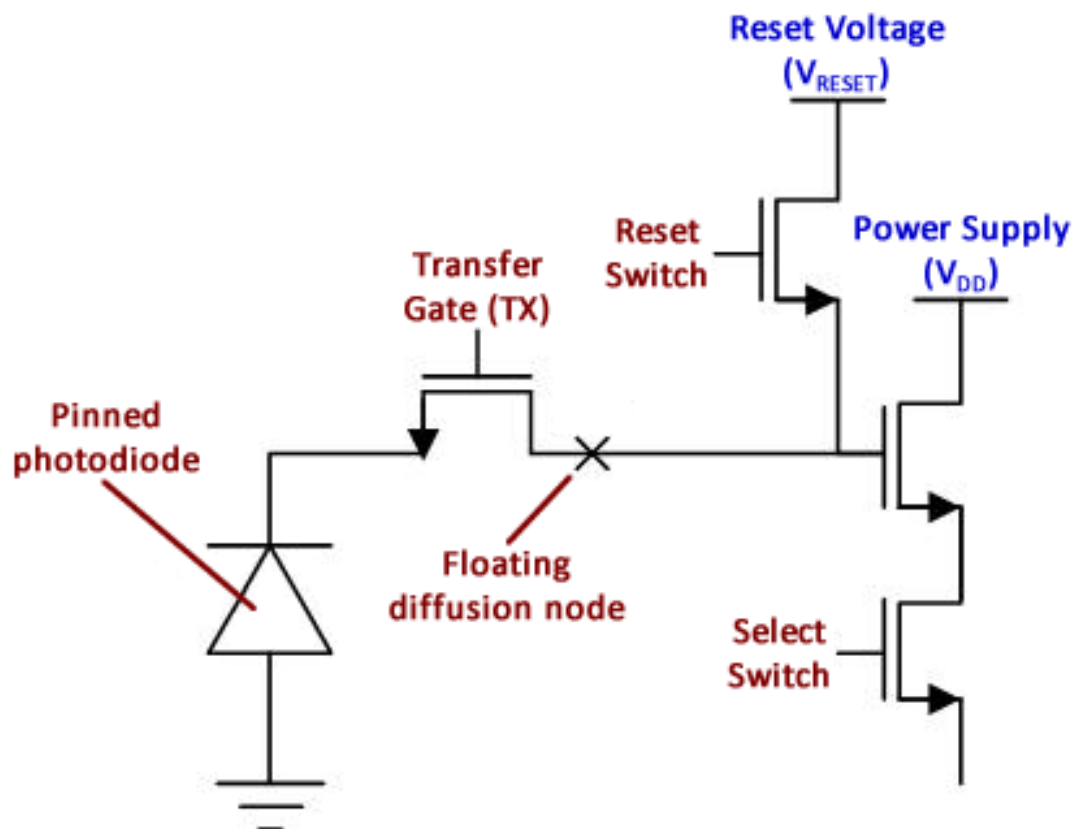
A photodiode lies in the photo-sensitive region of the pixel and collects charge proportional to the number of photons hitting its surface. Each row of pixels is connected to a select transistor that determines which row of pixels has been selected for read out at any one time. Once a row select transistor has been engaged, the pixel is reset via the reset transistor (which acts as a switch) and the charge accumulated by the photodiode during the light detection, or *integration*, period is buffered by a source follower transistor before being transferred to the column bus (a strip of metal connecting each pixel in a single column). This voltage is held in the column bus' *sample-and-hold capacitor* until it is time for that column bus to be read out. At this stage, the stored voltage is sent to one or more readout amplifiers to be taken off the chip.

Because the 3T pixel is an active pixel sensor (APS), there is an amplifier in each pixel, which means the total area of the pixel that is photo-sensitive is reduced. This lowers the pixel's *fill factor* (the percentage of the pixel occupied by the photodiode and any other unused space) compared to the simplest form of passive pixel sensor. An additional problem is that each amplifier will be slightly different, resulting in spatial offsets, known as *fixed pattern noise*, throughout the sensor. Fixed pattern noise is more pronounced vertically because of amplifiers in the column circuitry contributing additional noise.

One method of reducing fixed pattern noise is delta double sampling (DDS). In DDS, each pixel is sampled both before and after the integration period, which allows for the noise in the pixel electronics to be subtracted from the captured signal. However, this either requires two sample-and-hold capacitors in order to store both values, which results in more complex electronics, or it requires the first sample to be held off-chip for on-the-fly subtraction.

### (2.1a) 4T Pixels

A 4T pixel is a variation of the standard 3T pixel, aimed at solving various noise issues with 3T pixels (mainly kTC noise, see *Section 2.3b*). *Fig. 10* below shows the arrangement of a typical 4T pixel.



*Fig. 10 – 4T Pixel (adapted from <sup>[15]</sup>)*

A pinned photodiode is a photodiode with an extra thin p-type implant at its surface. Because of this, when a voltage (called the *pinning voltage*) is applied to the diode, two depletion regions form near the back-to-back diodes. When these two regions meet, the diode is emptied of charge. Since there are no electrons remaining on the diode, the transfer is noiseless.

In normal 4T operation, an integration period is completed, followed by the resetting of the separate readout node (known as the *floating diffusion node*). This reset value is then sampled before the transfer gate is opened in order to sample the signal value and empty the diode. This is known as *correlated double sampling* (CDS) and largely eliminates both fixed pattern noise and kTC noise because the noise from the floating diffusion node capacitance is read in both the signal and reset value, thus it is thus eliminated when the two signals are subtracted. CDS subtraction can be done either on or off-chip but either way, additional circuitry is required in each pixel, thus fill factor is again reduced.

## **(2.2) PERFORMANCE PARAMETERS**

Below an overview of the most important properties of a CMOS sensor that show how well it performs. There is often a compromise between these properties, so the design of the sensor is often heavily reliant on its intended application.

### **(2.2a) Fill Factor**

Fill factor is the percentage of the pixel that is photo-sensitive (known as the active region). The more electronics placed within a pixel, the lower the fill factor will be. Since CMOS sensors usually rely on 3 or more transistors and optionally a DAC within each pixel, the fill factor is always going to be less than 100% when it is front-illuminated. If the sensor is back-illuminated the fill factor can theoretically be 100% but this requires back-thinning, which is expensive and can introduce crosstalk.

## (2.2b) Full Well Capacity

Full well capacity or *maximum* full well capacity (MFWC) is the largest charge that can be stored in the photodiode. Thus, this is the highest detectable signal of the sensor and is given by:

$$4 \quad q = CV$$

$C$ , the photodiode capacitance (floating diffusion capacitance for 4T pixels), is fixed (and includes the parasitic capacitance) and  $V$ , the voltage, is defined by the reset level and limits of the readout circuitry. Because the maximum detectable signal is not by itself very useful, another property known as the *linear full well capacity* (LFWC) is also defined as the maximum signal value that can be obtained whilst retaining a linear response. This value is obtained from a photon transfer curve (see *Section 2.5*).

## (2.2c) Conversion Gain

The conversion gain of a sensor is the number of  $\mu\text{V}$  per electron measured at the output and defines the sensitivity of the pixel to small amounts of charge in the voltage domain <sup>[15]</sup>. The reason the output signal is not identical to the number of electrons is that the voltage is amplified various times throughout its readout path. Conversion gain, usually given by the symbol  $K$ , can be found using the following formula:

$$5 \quad K = \frac{q_e}{c} \times K_{AF}$$

(where  $q$  is the charge of an electron,  $K_{AF}$  is the gain from the pixel node to the output of the chip, which includes the source follower, and  $c$  is the parasitic and diode capacitance for 3T pixels or parasitic and floating diffusion capacitance for 4T pixels)

Parasitic capacitance is the capacitance of an electrical circuit that exists simply because of components' proximity to each other. Conversion gain can be calculated from a log-log photon transfer curve (see *Section 2.5* and *Equation 17*).

## (2.2d) Quantum Efficiency

Quantum efficiency is the number of electrons produced compared to the number of incident photons on the pixel. It includes the fill factor and other losses related to the different material layers within the surface of the sensor. It is a measure of how responsive the sensor is to different wavelengths of light and is calculated as follows:

6

$$QE = \frac{\eta_i P_i}{P}$$

(where  $\eta_i$  is the quantum yield gain,  $P$  is the average number of incident photons on the pixel,  $P_i$  is the average number of incident photons that interact in the pixel)

Quantum efficiency is mainly dependent on the size of depletion region and fill factor. The easiest way to obtain a value for quantum efficiency is to plot a graph of dark-corrected signal against incident photons and use the gradient in the following equation:

7

$$QE = \frac{m}{K}$$

(where  $m$  is the gradient of the dark-corrected signal against incident photons graph and  $K$  is the conversion gain)

The number of incident photons can be calculated if the power per unit area output by the light source being used is known:

8

$$N_\gamma = \frac{\lambda t I A}{h c}$$

(where  $\lambda$  is the wavelength of the incoming photons,  $t$  is the integration time,  $I$  is the intensity of the incoming photons ( $\text{Wm}^{-2}$ ),  $A$  is the pixel area,  $h$  is Planck's constant and  $c$  is the speed of light)

## (2.2e) Dark Current

When no light is incident on the active region, there would be no current flow in an ideal sensor. However, in real sensors, there is a small leakage current, known as *dark current*, produced from thermally generated charges. In the case of 4T pixels, dark current is believed to be dominated by the transfer gate <sup>[17]</sup>.

The dark current of a single pixel can be determined by taking the signal read from that pixel when the sensor is not exposed to light. If this can be done with several integration times then

the dark current per second can be calculated. If the dark current is known, then the signal from each pixel can be “dark corrected” to produce a signal response graph that extrapolates to zero. Because dark frames are dominated by kTC noise, the variances of dark these frames can be used to calculate the readout noise of the sensor.

### **(2.2f) Dynamic Range**

Dynamic range is, in simple terms, the ratio between the smallest and largest possible values read out from the sensor. However, a more accurate and realistic value for dynamic range can be obtained from a photon transfer curve (see *Section 2.5*). It is defined as the signal value at the peak of the PTC (full well capacity) minus the readout noise value (which can also be obtained using a PTC).

The higher the dynamic range of a pixel, the greater the signal resolution is (assuming fixed minimum and maximum detectable light levels). Dynamic range is related to the signal-to-noise ratio of the pixel. An active pixel sensor has various noise sources, some of which are described below.

### **(2.2g) Image Lag**

Image lag is defined as the proportion of charge in subsequent dark frames from a single bright frame. In essence, the signal from the pixel is not completely drained and so part of it remains and becomes part of the signal captured during the next integration period.

In a 3T pixel, this is usually due to an insufficient reset method being used (see *Section 2.3b* for more details). For 4T pixels, if the transfer gate doesn't operate correctly or isn't enabled for long enough, excess charge can remain on the diode, causing image lag. For this reason, image lag can be referred to as *charge transfer efficiency* in the case of a 4T pixel.

The effect of image lag can be seen in normal cameras as ghosting or blurring. It is especially problematic in high speed environments but not as much in applications such as particle physics where the camera is usually still and the charges involved are small. However, it is desirable for the built-up charge to be read out as quickly as possible so the efficiency of transferring charge from the diode to the floating diffusion node is important (see *Fig. 10*).

## (2.2h) Dark Signal Non-Uniformity and Photon Response Non-Uniformity

These two properties describe the uniformity of each pixel in an array. Dark Signal Non-Uniformity (DSNU) tells us the distribution of dark current, whereas Photon Response Non-Uniformity (PRNU) tells us the pixel responsiveness when illuminated <sup>[10]</sup>. Both distributions are measured in the same way, using *Equations 9 and 10* below, with the former in the dark and the latter in the light.

9

$$DSNU = \frac{\sigma_{DM}}{S_{DM}}$$

( $\sigma_D$  is the square root of the variance of the mean of various dark signal values,  $S_D$  is the average dark signal (ideally calculated from a dark current graph))

10

$$PRNU = \frac{\sigma_{DCM}}{S_{DCM}}$$

( $\sigma_{DC}$  is the square root of the variance of the mean of various dark-corrected signal values,  $S_{DC}$  is the average dark -corrected signal)

These values should be calculated for every integration time in an integration sweep. When plotted against integration time, DSNU would ideally produce a straight horizontal line, whereas

PRNU will not. Due to the fact that it is difficult to analyse and quantify these parameters, and that the ability to calculate these parameters was only implemented at the very end of the research year, these calculations were not done for this project.

## (2.3) NOISE

The noise of a sensor is important when detecting low-level radiation because it dictates the minimum detectable signal. There are three main types of noise associated with CMOS image sensors, which are discussed below. Other noise sources exist, such as ADC noise, but they are either negligible or difficult to control or measure, so they are not included in our sensor tests.

### (2.3a) Photon Shot Noise

The number of photons hitting a pixel and the thermally generated charges within the pixel fluctuate according to Bose-Einstein statistics:

$$\sigma(P_i)^2 = P_i \frac{e^{hc/\lambda kT}}{e^{hc/\lambda kT} - 1}$$

Since, at room temperatures and with photons near the visible part of the spectrum,  $hc/\lambda \gg kT$ , this approximates to:

$$\sigma(P_i)^2 = P_i$$

$$\sigma(P_i) = \sqrt{P_i}$$

( $P_i$  is the average number of incident photons that interact in the pixel)

This noise relation is the same as that for a Poisson distribution. Because the electrons comprising the signal are created by these incoming photons and thermally generated charges, the shot noise in the signal is simply given by:



13

$$\sigma(S) = \sqrt{S}$$

Shot noise is the main noise factor at medium to high light levels and is the main limitation of the signal-to-noise ratio and dynamic range of the sensor. Because shot noise has a fixed theoretical limit, the only way to reduce it is to increase full well capacity (i.e. increasing the maximum  $N$  detectable). Photon shot noise is the basis for the *photon transfer curve* (see *Section 2.5*).

### (2.3b) Reset Noise

The source of reset noise (also known as *kTC noise* because it varies with the Boltzmann constant, temperature and capacitance) is random fluctuations in voltages read from the capacitors in each pixel. Reset noise can be reduced using different reset techniques. The simplest, and least noisy, method is known as *soft reset*. This involves setting the gate-to-drain voltage ( $V_{GD}$ ) of the reset MOSFET to be lower than its threshold voltage ( $V_{Th}$ ), resulting in a reset noise of:

14

$$\sigma_{soft\ reset} = \sqrt{\frac{kTC}{2q}}$$

A diagram showing a soft reset is in *Fig. 11*. The reset transistor is in *weak inversion* and unidirectional movement occurs between diode and reset voltage node.

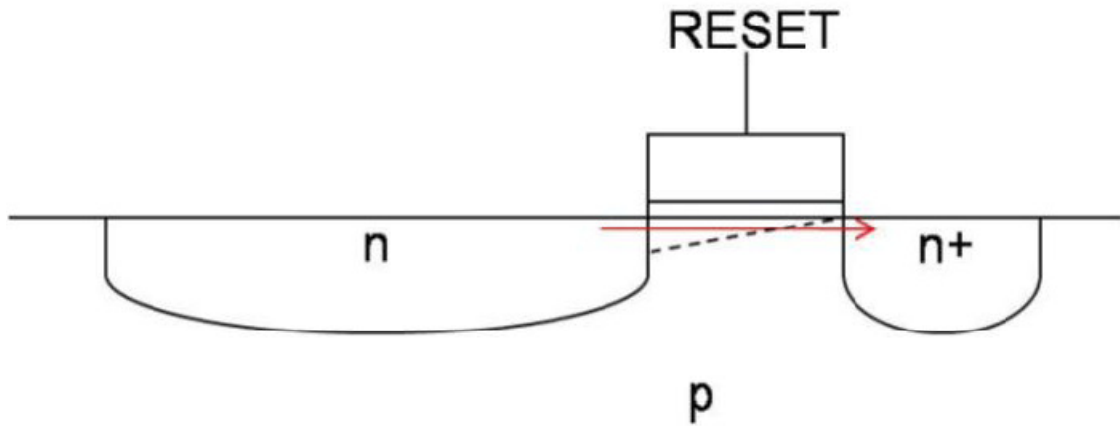


Fig. 11 – Soft reset<sup>[7]</sup>

The disadvantage of this method is that it introduces image lag (see Section 2.2g). If VGD is set higher than  $V_{Th}$ , known as hard reset, the pixel's signal is fully cleared and the pixel does not suffer from image lag. However, because bidirectional movement can occur between diode and reset voltage node, as shown in Fig. 12, noise increases by a factor of  $\sqrt{2}$  also:

15

$$\sigma_{hard\ reset} = \sqrt{\frac{kTC}{q}}$$

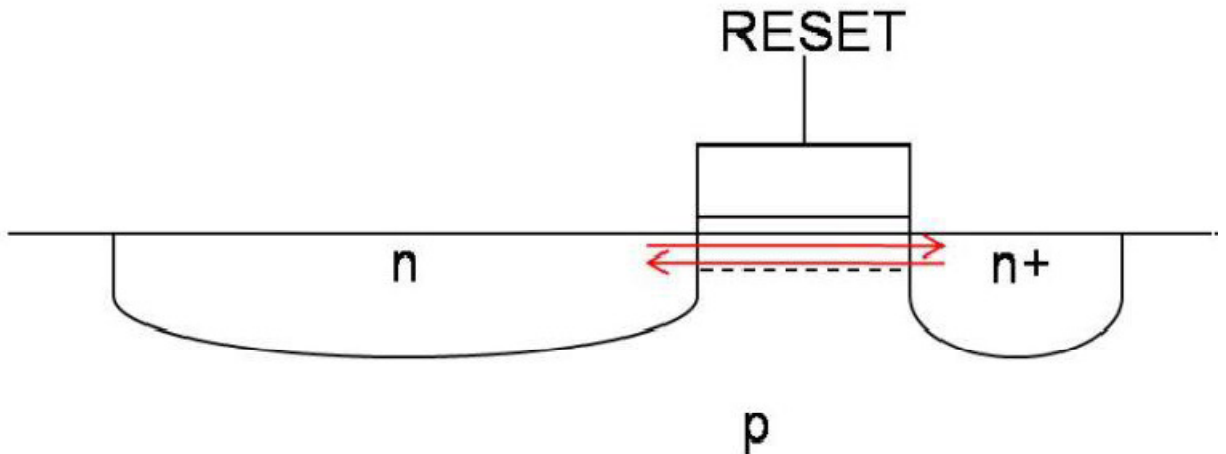


Fig. 12 – Hard reset<sup>[7]</sup>

Since reset noise is not dependent on the number of interacting photons, it is only dominant at low signal levels, being taken over by shot noise with higher photon counts. *Correlated double*

*sampling*, as discussed in the *Section 2.1a*, helps reduce reset noise since it is sampled both with and without the signal.

### **(2.3c) Fixed Pattern Noise**

As mentioned before, the fixed pattern noise of a sensor arises from the minor differences or imperfections in the electrical components in each pixel and produces a spatially static noise pattern on the sensor. It is again not dependent on the number of interacting photons so is only a dominant noise source at low light levels. In 4T pixels, *Correlated Double Sampling* makes this noise negligible.

Thus, when CDS is used, the sensor is left essentially *shot noise limited*, which is the ideal situation in terms of noise. However, these noise reduction techniques have other consequences such as reduced fill factor and increased cost, so there is always a compromise.

### **(2.3d) Random Telegraph Signal Noise**

When viewing the direct output of a normal 3T sensor on an oscilloscope, you would see the signal flicker between two discrete levels. The cause of this is thought to be random telegraph signal noise (RTS noise) <sup>[19]</sup>. Knowledge of this type of noise is limited but what is known is that it is proportional to the reciprocal of the frequency; hence it is often referred to as *1/f noise* <sup>[11]</sup>. There are some experimental techniques aimed at improving RTS noise in CMOS sensors, including altering the shape and size of the source follower. When viewing a noise histogram, the occasional unusually high values are typically caused by RTS noise.

## **(2.4) RADIATION DAMAGE**

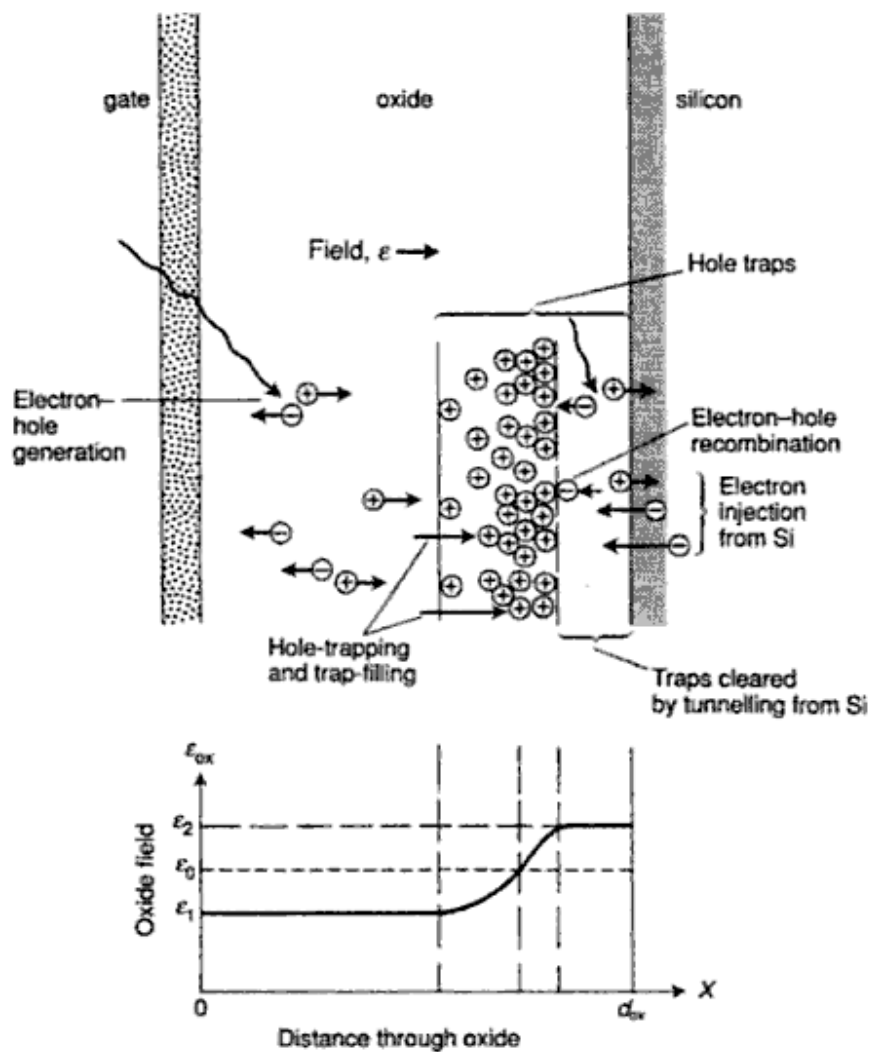
There are two types of radiation that will be incident on CMOS sensors when used in most common scientific applications, such as x-ray detection or particle physics. Radiation can be ionising or non-ionising. Non-ionising radiation includes particles such as neutrons or protons, whilst ionising radiation includes electromagnetic waves and charged particles such as electrons or protons. Although CMOS image sensors are less susceptible to radiation damage than CCDs due to their thinner oxides <sup>[13]</sup>, both types of radiation cause degradation to the performance of the sensor, so it is important to discover how much the sensor is affected by certain doses and whether it can recover from such exposure.

Non-ionising radiation (which causes “bulk damage”) should only affect charge collection within the pixel and not any of the CMOS electronics. However, it is not possible to perform tests with non-ionising radiation in a laboratory environment due to safety regulations and lack of access to such a source. Therefore, investigation of the effects of non-ionising radiation is beyond the scope of this project. Access to ionising radiation in the form of high energy electromagnetic waves such as gamma rays and x-rays is much easier, and for this project, x-rays were the chosen source. To introduce the type of damage induced by x-rays, only ionising radiation will be discussed in detail from now on.

### **(2.4a) Ionising Radiation**

Ionising radiation causes the valence band electrons to be elevated into the conduction band and to become highly mobile if an electric field is applied. The positively charged holes are also

mobile but to a lesser degree. Because of this, ionisation in the oxide, combined with traps present due to defects in the oxide, causes trapped holes. Trapped charge has its own electric field associated with it and can alter a solid's conductivity, and in the case of MOS, alter the  $V_{Th}$  of the transistor due to the change in the formation of the conductive channel from the trapped positive charge. Thus, the production and trapping of these holes in oxide films causes degradation in MOS devices. A diagram showing this effect is seen in *Fig. 13* below:



*Fig. 13 – The formation of trapped holes in MOS.* <sup>[8]</sup>

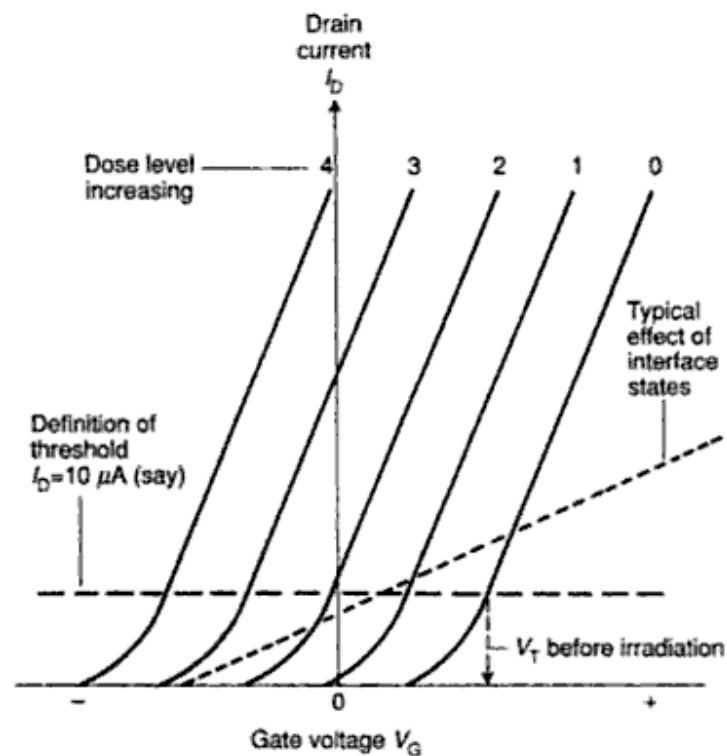
Because no momentum transfer to atoms is involved in creating these electron-hole pairs, the energy of the incident radiation is not important (as long as it is high enough to create an electron-hole pair, which in silicon dioxide is  $\sim 18\text{eV}$  <sup>[18]</sup>). This is useful for testing the tolerance of devices to ionising radiation for applications where particle detection is involved because ionisation effects produced by particles in the MeV range can be simulated using much lower energy gamma rays or x-rays. Ionising radiation exposure is measured either in *rads* (radiation absorbed dose) or *grays* ( $1\text{ Gy} = 100\text{ rad}$ ).

It is important to note that the amount of charge trapped due to ionising radiation depends strongly on the voltage across the oxide during irradiation. There are five main irradiation biases to consider:

- 1)  $V_i +$ : Positive voltage applied to the sensor
- 2)  $V_i -$ : Negative voltage applied to the sensor
- 3)  $V_i 0$ : Sensor shorted to ground
- 4) Floating: Sensor not biased
- 5) Sensor operating in normal conditions (clocked)

Cases (3) and (4) are markedly different because a floating voltage can be slightly negative or positive, which will affect the radiation damage. In order to realistically test a sensor's tolerance to radiation whilst in normal use, it must be operating in normal conditions (i.e. biased or clocked). Various standards exist for how to reliably test image sensors and ICs with radiation, such as the ESA standard. <sup>[9]</sup>

To summarise, the consequence of radiation exposure is physical change in the MOS devices, at the interface and in the isolating oxide layers within the sensor. This causes the progressive loss of function of such MOS devices, as well as eventual failure of the MOS circuits. *Fig. 14* below shows how the change in drain current flowing in the channel with respect to the gate voltage of a CMOS device varies with progressively higher doses of radiation:



*Fig. 14 – Typical  $I_{DS}$ - $V_{GS}$  curves for an NMOS device after radiation damage failures.* <sup>[8]</sup>

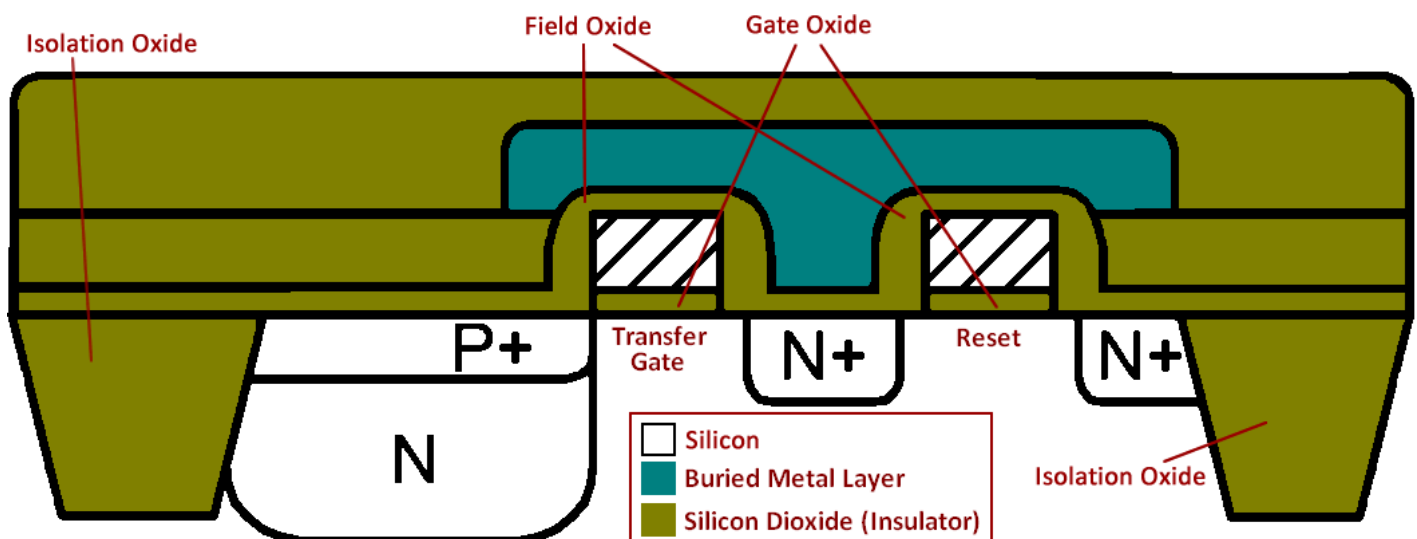
## (2.4b) Effect of Trapped Charge on NMOS Transistors

The 4T pixels investigated in this project contain just NMOS transistors (no PMOS transistors) so the specific effect on them is important. Trapped holes induced by ionisation in the oxide layer of an NMOS transistor will have the same effect on the silicon as applying a positive gate voltage. The energy bands will be bent downwards and will tend to induce inversion in the p-

type substrate. The reason that the threshold voltage will decrease is that the trapped holes repel positive charge, leaving behind negative ions to form a channel underneath the oxide which exists regardless of an applied voltage. Therefore, a lower positive voltage is required to form a channel, so the n-type conductivity of the NMOS is increased. If the number of trapped holes is high enough, inversion may be established without the addition of a gate voltage, causing leakage current in the off state of the transistor.

#### (2.4c) Effect of Interface States on CMOS Image Sensors

Fig. 15 below shows a cross-section of a typical 4T CMOS image sensor:



*Fig. 15 – Typical CMOS sensor cross-section diagram.*

Modern processing techniques can help greatly reduce the observable defects of interface states. For example:

- 1) Higher quality production of silicon dioxide, with fewer defects.
- 2) Thinner gate oxides which scale with smaller technologies (so trapped holes have a higher chance of tunneling out or being annihilated by tunneling electrons).

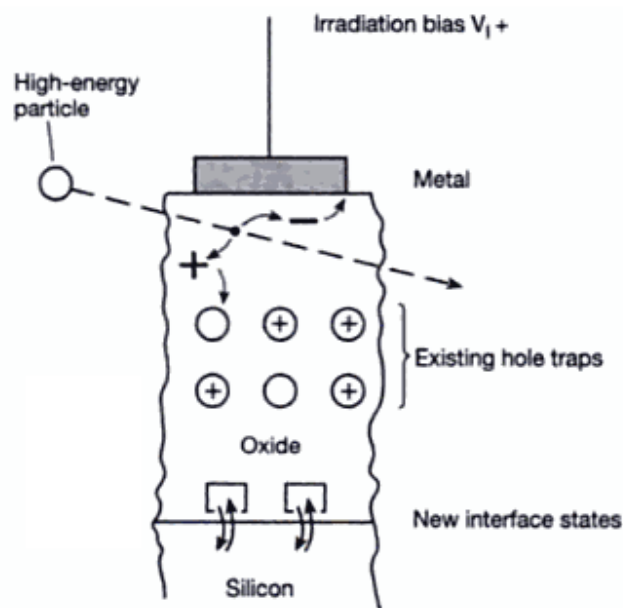


3) Different materials may be used for isolation.

However, even with these improvements, radiation exposure can still cause ionisation to occur within the thick field oxide (silicon oxide) and over the top of the diode, where the trapped holes have less chance of tunnelling free.

Wherever silicon meets silicon dioxide, interface traps are produced due to the change in structure between the two materials. Interface traps have similar effects to traps within the oxide, although the traps themselves have different characteristics (such as a longer lifetime).

*Fig. 16* below shows the location of interface states in a CMOS device:



*Fig. 16 – Typical formation of new interface states.* <sup>[8]</sup>

In CMOS image sensors, interface states occur in the field oxide and over the top of the diode (see *Fig. 15* above). Not only are the electronics in the pixels affected by radiation exposure but the readout circuitry (including the row and column addressing logic) are also affected. Results from radiation exposure tests generally show that the performance of CMOS image sensors start

to be affected by radiation in the 1 kGy range and tend to seriously degrade and become unreliable in the 10 kGy range. <sup>[8]</sup>

Expected changes in sensor performance include an increase in dark current and noise (see *Sections 2.2e and 2.3*). It has been suggested that the likely failure modes for CMOS image sensors include *offset fixed-pattern noise* arising from non-uniform ionisation in the oxides (see *Section 2.3c*). The noise will eventually become so high that the sensor will not be able to detect any signal.

#### **(2.4d) Annealing**

After being exposed to radiation, a MOS device will gradually recover over time unless it has been irreversibly destroyed by radiation damage. This is because applied fields, or fields induced by positive trapped charge, can attract electrons to annihilate the trapped holes, allowing the device to return to its previous pre-irradiated state. The ESA specification specifies to keep the sensor biased in the same way during irradiation and annealing. <sup>[9]</sup>

Lower temperatures will greatly slow down this recovery process, which is useful for preventing unwanted annealing that could produce misleading results during testing (for example, when investigating the maximum amount of radiation exposure the sensor can handle. On the other hand, high temperatures will significantly speed up annealing, which can be useful for finding out whether a sensor can recover over a long period of time after an extended period of low-dose-rate exposure (e.g. a total dose of 10 kGy over the course of a year). The ESA specification also details this. <sup>[9]</sup>

## (2.5) PHOTON TRANSFER CURVE

A *photon transfer curve* (hereafter referred to as “PTC”) is obtained from a graph by plotting the RMS noise against the dark-corrected signal. This can be done for an individual pixel or it can be for each pixel averaged together to get a PTC for the entire sensor. In order to be able to produce a PTC, various image captures (*frames*) are needed for a number of different photon exposures. This can be done by taking images using a fixed integration time and gradually increasing the light level or the light level can be fixed and the integration time can be changed. In general, varying the intensity (*intensity sweep*) takes less time to do but it has one flaw – the dark current cannot be assessed (this requires *dark frames* to be taken with various integration times) – so it cannot be used in all situations.

There are two ways of analysing data to create a PTC. The first is taking two frames at each intensity/integration time and looking at the spatial variation of the pixels in each. The second is to take many frames to investigate per-pixel temporal variations.

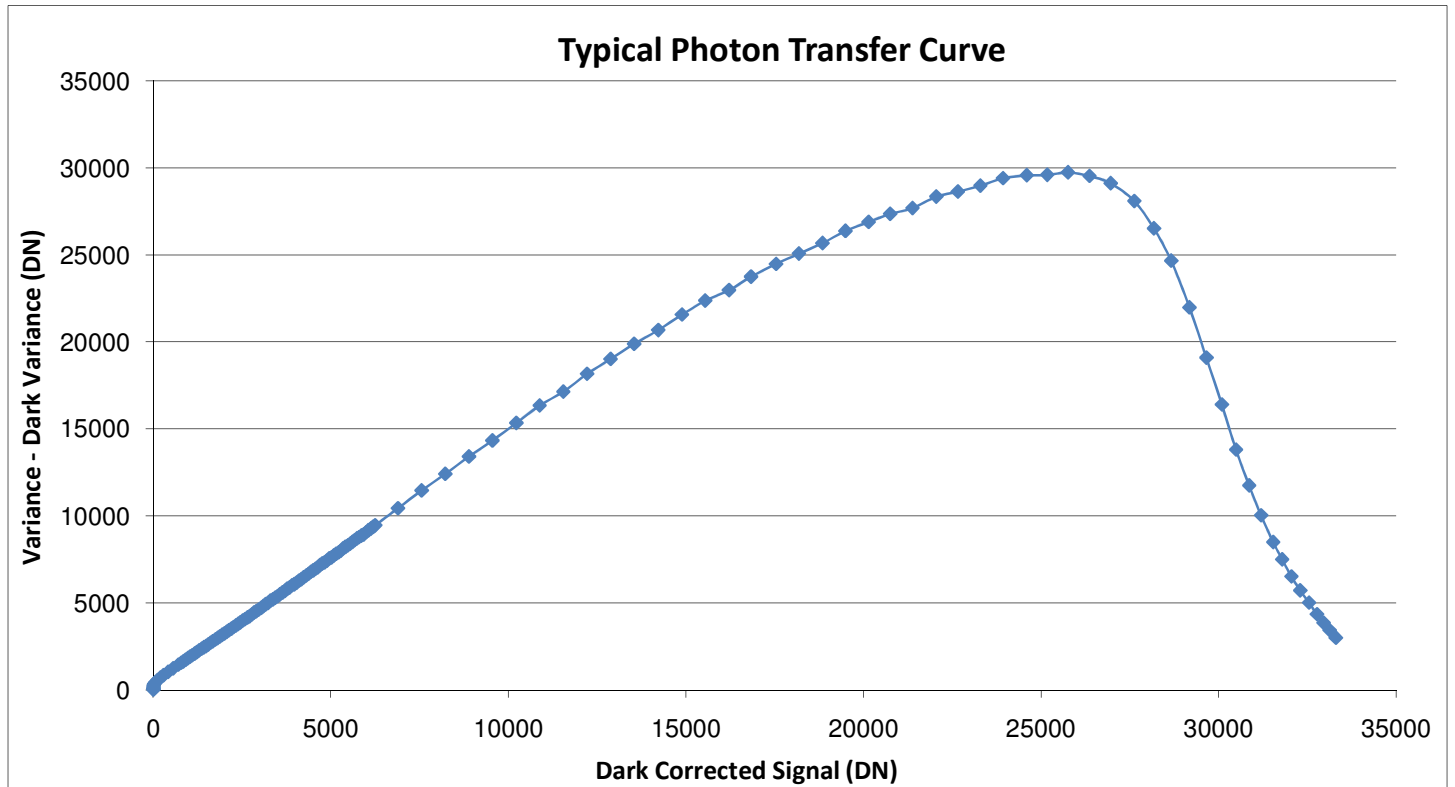
In order to obtain the *dark-corrected signal*, several dark frames should be obtained, averaged, and then subtracted from each *light frame* taken. The RMS noise of a single frame can be calculated from the standard deviation of its pixel values (after dark correction):

16

$$\sigma_{Frame} = \sqrt{\left( \frac{\sum_{i=1}^{N_{pixels}} [S_i - S]^2}{N_{pixels}} \right)}$$

(where  $n$  is the number of pixels in the frame,  $S_i$  is the signal value of the  $i^{th}$  pixel in the frame,  $S$  is the average

The more pixels used and the more light intensities/integration times that are tested, the more reliable and accurate the PTC will be. A typical PTC is shown below:



**Fig. 17** – Typical photon transfer curve (taken from a real FORTIS set of results)

The “peak” of the PTC (in this case at approximately 25000 digital numbers) is the linear full well capacity of the sensor (see *Section 2.2b*). When a PTC is plotted on a log-log scale, it is easier to identify each distinct section of the curve, as shown in *Fig. 18* below.

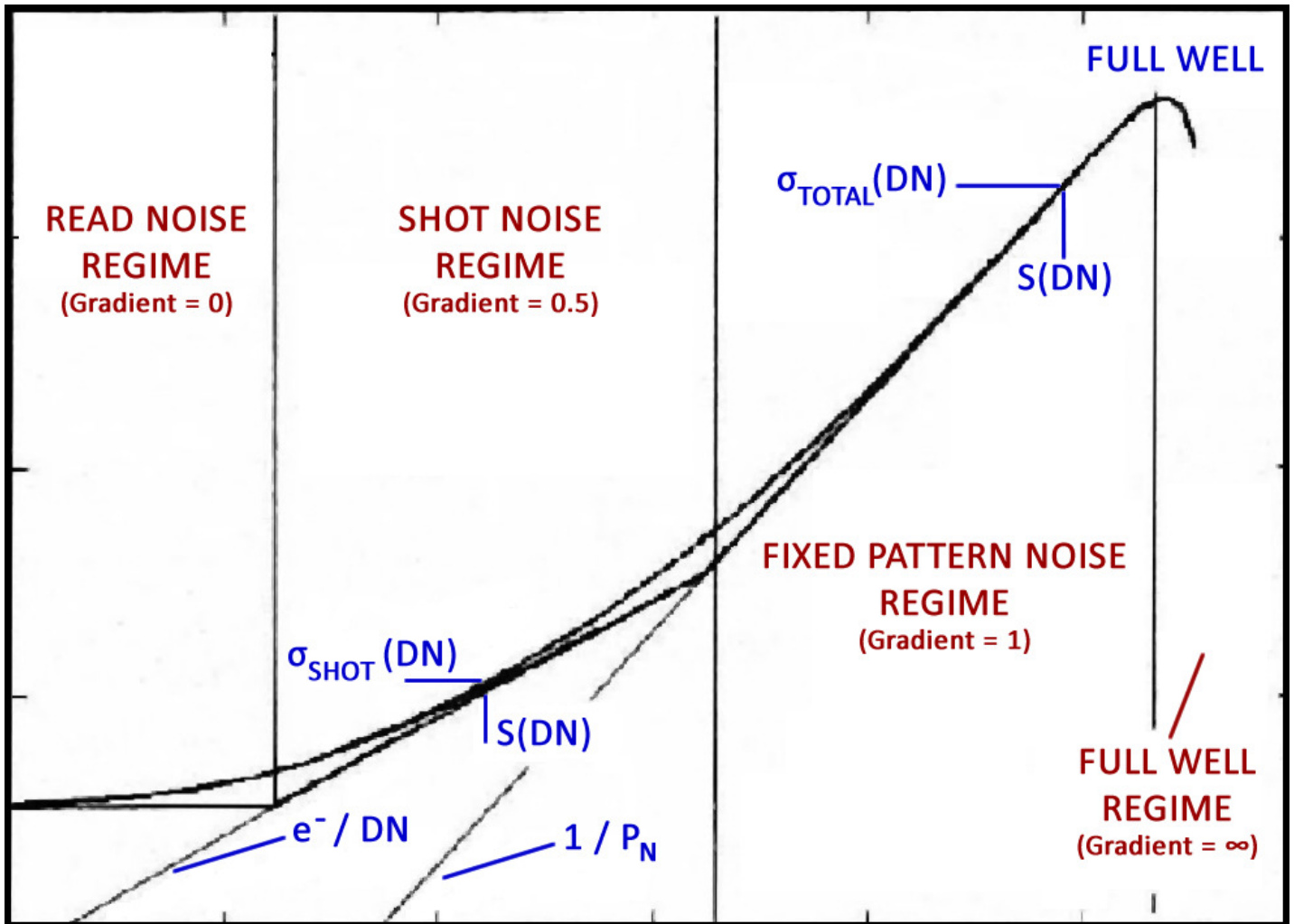


Fig. 18 – Typical log-log photon transfer curve <sup>[1]</sup>

The PTC has four distinct regions. The first is the read-noise section, which determines the minimum noise floor of the sensor. The second is the shot-noise section, which has a gradient of 0.5 on logarithmic scales. A best-fit line for this portion of the graph can be used to find the gain (K, in digital numbers per electrons) of the sensor using the following formula:

$$K = 10^{c/m} \quad (\text{where } c \text{ is the y-axis intercept, } m \text{ is the gradient})$$

The third section contains the sensor's fixed pattern noise. The gradient of this portion of the graph is 1. This section of the PTC does not exist for sensors that employ techniques to eliminate

fixed pattern noise. There is also a way of removing fixed pattern noise from a normal 3T sensor.

This involves taking the difference of two frames taken one after the other at the same light

level. Doing this causes random noise to increase by  $\sqrt{2}$  so this must be compensated for in the

result of this subtraction:

$$18 \quad \sigma_{without FPN} = \sqrt{\left( \frac{\sum_{i=1}^{N_{pixels}} [S_{1,i} - S_{2,i}]^2}{2N_{pixels}} \right)} \quad \text{(where } n \text{ is the number of pixels in the frame, } S_{1,i} \text{ is the signal value of the } i^{th} \text{ pixel in frame 1, } S_{2,i} \text{ is the average signal value of the } i^{th} \text{ pixel in frame 2)}$$

The final segment of the graph shows the full well capacity of the sensor, the point at which the

pixels can no longer linearly collect more charge. Hence, this is the maximum detectable signal

(and can be used for determining dynamic range).

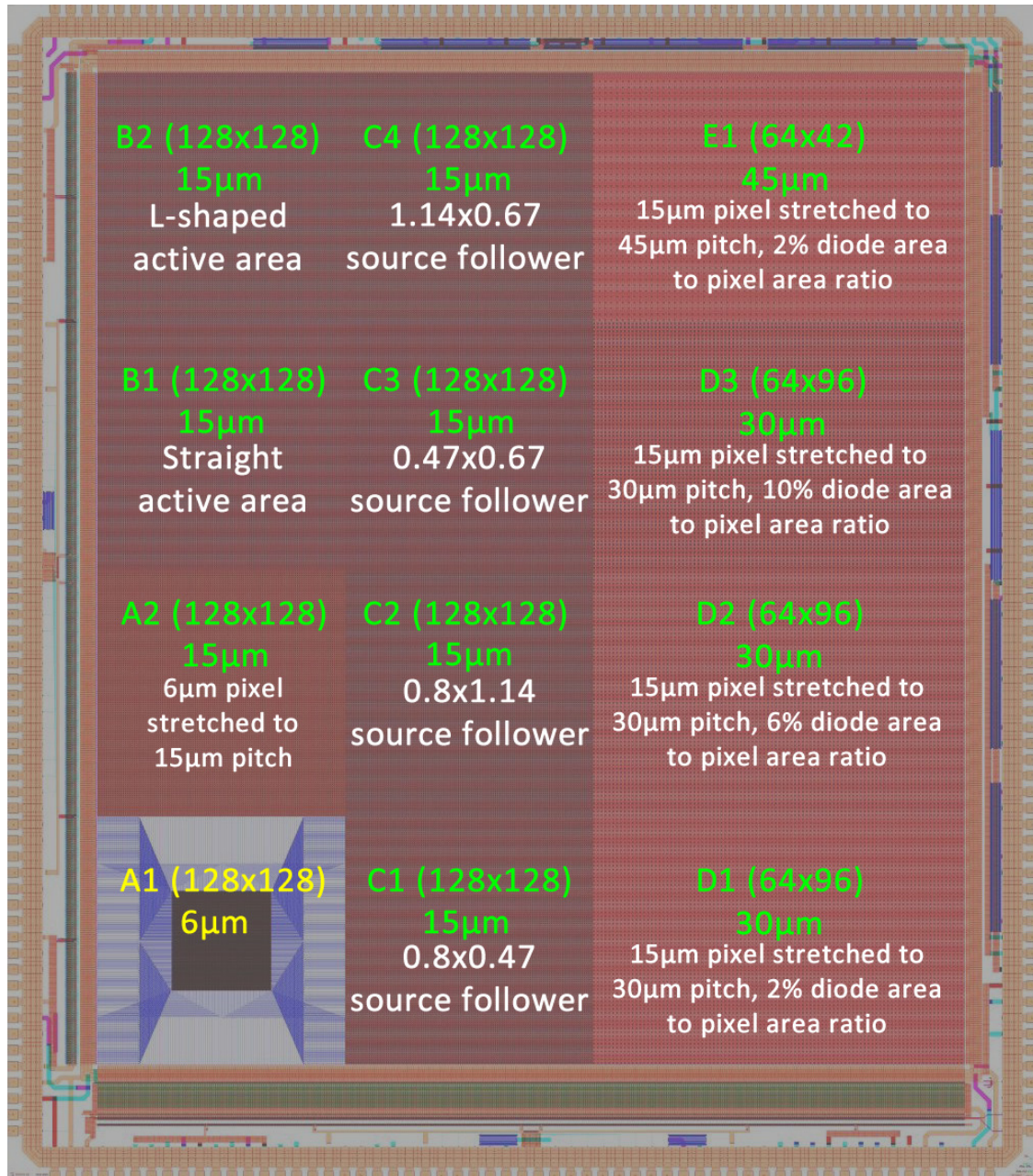
### **(3) EXPERIMENTAL METHOD**

#### **(3.1) SENSOR DESIGN**

The main task of my research year project was to test (including optimising and characterising) a sensor called FORTIS (**4T Test Image Sensor**). Its design was based on its direct predecessor eLeNA (**Low Noise Active Pixel Sensor**). FORTIS is a test chip for the group and is the first 4T sensor developed at RAL. It is designed for low noise applications (because it implements CDS) and it also has a high sensitivity to small charge due to its high conversion gain.

##### **(3.1a) FORTIS 1.0**

FORTIS 1.0 contains twelve different types of pixel, arranged in a grid, as shown in *Fig. 19* below. They differ in four main areas, with the goal of furthering the group's understanding of 4T pixels and finding the best layout for certain applications. These areas are: pixel size, diode size, active area shape and source follower transistor size.



**Fig. 19** – FORTIS 1.0 Pixel Types (adapted from<sup>[6]</sup>)

The standard pixel size is 15 µm, with the other pixel sizes being made using a compromise of this structure. The shape of the active area was altered based on consultation with the foundry. The default pixel design has an L-shaped active area with a large floating diffusion node. The resulting capacitance is ~5fF, producing a low conversion gain<sup>[6]</sup>. In order to decrease this



capacitance (and therefore increase conversion gain), the floating diffusion node was decreased in size and the distances between the transistors was reduced in one modification. One variation is a straight active area with straight metal lines connecting it to the gates of the transistors. In theory, this should reduce parasitic capacitance.

Source follower shape and size is important because it has been reported that the temporal noise of the source follower is the limiting factor in image quality. Three width/length ratios were tested with FORTIS 1.0 in the “C” pixels: 0.7, 1.2 and 1.7. These differently sized source followers could have an effect on random telegraph signal noise (see *Section 2.3d*).

Diode size variations were tested with the 30 $\mu\text{m}$  “D” pixels, using diode area to pixel area ratios of 2%, 6% and 10%. The last pixel, E1, uses the standard 2% ratio on a 45 $\mu\text{m}$  pitch.

Each sensor was manufactured using three different processing variations, two of which differ from the standard control batch (*processing variation 1*, which has the same implants as the foundry’s original 6 $\mu\text{m}$  pixel) in order to test additional techniques to improve sensor performance. *Processing variation 2* has an increase in diode implants to increase the pinning voltage by 0.3V. *Processing variation 3* has an increase in N doping of the diode whilst keeping the pinning voltage constant. It was predicted that processing variation 2 would provide the best overall performance.

### **(3.1b) FORTIS 1.1**

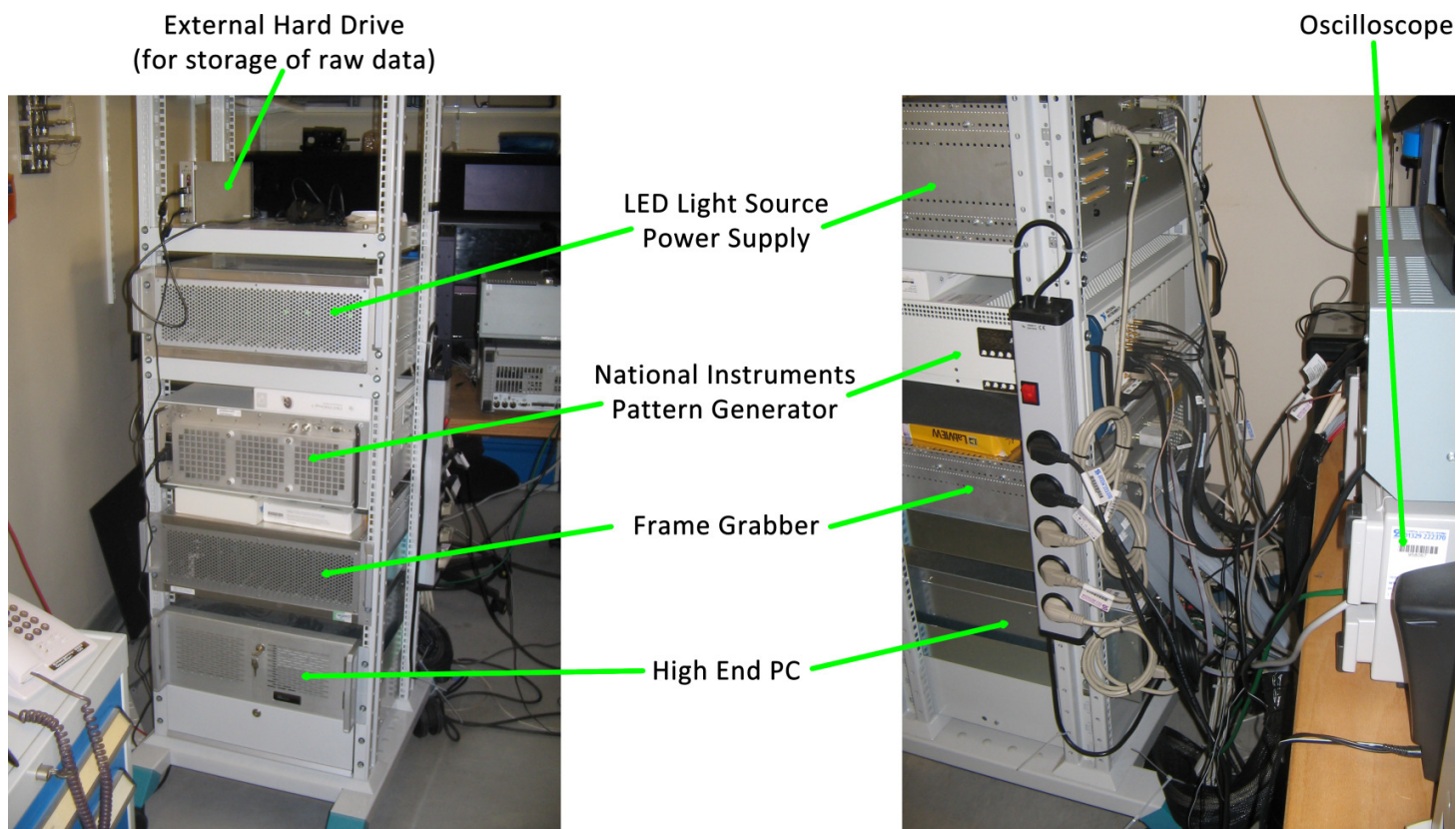
A revised version of FORTIS 1.0, named FORTIS 1.1, was created using different implants in the hope of reducing source follower noise <sup>[15]</sup>. The opportunity for redesign was also used to implement a 13<sup>th</sup> pixel variant, D1-bin, which is a 64x48 array located in between the C1 and D1 pixel arrays, reducing the original D1 pixel array to 64x48. Each D1-bin 30µm pixel is essentially four 15µm pixels tied together at the floating diffusion node, creating a “binned” pixel where the charge from four diodes is combined. Due to the increase in floating diffusion capacitance, the conversion gain should decrease, alongside an increase in noise. Other improvements were made in order to attempt to further reduce the noise of certain pixels and the chips were manufactured using seven different processing variations incorporating advanced CMOS techniques such as *deep P-well* and *high-resistivity substrates*.

### **(3.2) SENSOR TESTING**

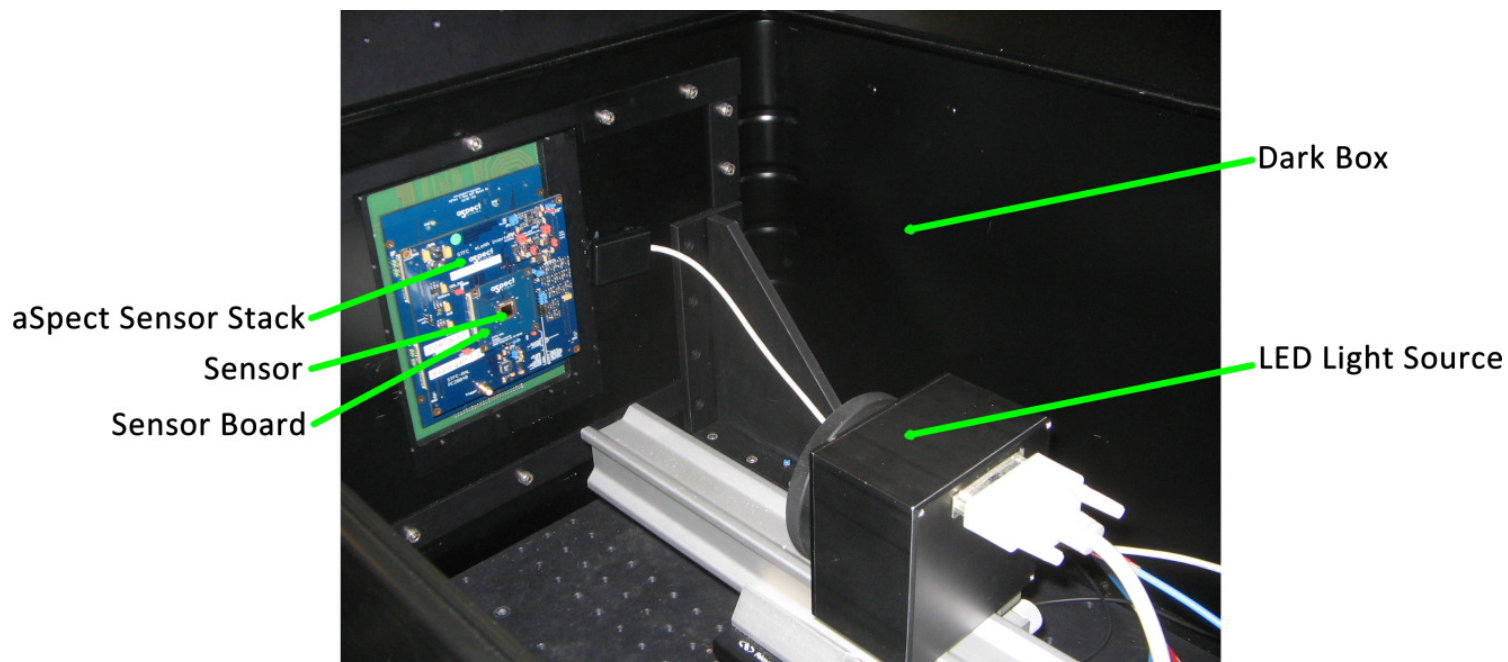
FORTIS was tested using a customised test system built by aSpect, which is the most comprehensive testing system available to the CMOS Sensor Design Group.

#### **(3.2a) The aSpect System**

RAL currently owns two of these systems, both of which reside in the CMOS Sensor Design Group’s optics lab. They differ slightly in their configuration but their operation is essentially the same. They consist of a dark box, a pattern generator (National Instruments PXI 6561), a frame grabber (NI 1429e) using a Single or Dual Full Camera Link (up to 10Gbps, allowing for very fast frame rates and/or very large image sizes), as well as a calibrated LED light source.



*Fig. 20 – aSpect Test System Rack (Tester 1 shown)*



*Fig. 21 – aSpect Test System Dark Box (Tester 1 shown)*

All of these components are connected to a high-end PC via PCI-Express cards and are controlled by custom written LabVIEW software called *idVIEW*. The LED light source can operate in four modes: blue (470nm), green (546nm), red (635nm) and infrared (850nm). The infrared mode is disabled on *tester 1*. The light source must be calibrated using a photodiode for optimum performance. This can be done within *idVIEW* in approximately 30 minutes and is currently performed every couple of months. It is used with a lens requiring a distance of 35cm to the sensor. This is checked every time a calibration is done.

In order to test a sensor, vectors, which define both the area of the chip to be read out and the status of various control switches throughout an integration cycle (such as reset and read out switches), must be generated and applied to *idVIEW*. Once all of the system components have been initialised, the vector is sent to the pattern generator and is used to run the sensor. Images can then be grabbed either one at a time or continually and saved for future reference.

The main testing methods used on the aSpect system are the *intensity sweep* and the *integration sweep*. The former method grabs a set number of frames (typically 100) with a specific integration time (defined by the vector used) at various intensities. The latter method involves grabbing both a set of dark frames (with the light source off) and a set of light frames (with the light source at a pre-defined level) with various integration times (again, typically 100 of each).

### **(3.2b) Pixel Optimisations**

Each pixel type on FORTIS 1.0 was optimised in two ways. Firstly, the timing of the four main switch commands was optimised for dynamic range and noise. These switches are the signal sample (Sample S), the reset sample (Sample R), the reset switch (Reset) and the transfer gate (TX). It was also found that switch timings had an insignificant effect on noise but a measurable (albeit small) effect on dynamic range, which can be calculated simply by taking the average result of a frame captured with both no light and at saturation. Thus, sweeps were not needed to optimise vector timings. Further tests confirmed that our use of a minimal gap between these commands produced the best dynamic range results and also reduces signal degradation in the floating diffusion node to a minimum.

*Fig. 22* shows an example of the final optimised timings for the B2 pixel on processing variation 2. Each bit in the sequence represents 1 $\mu$ s. Each D\_Y\_PAD and D\_X\_PAD signal is a column and row select switch. These are automatically configured by our vector generator depending on which rows and columns are selected to be read out and so do not need to be set manually in the pattern sheet. Note that the integration time is defined as the time between the end of one TX signal to the beginning of the next TX signal.



The second optimisation technique involved tweaking voltages. Five separate voltages were changed in order to find the optimum setup for the pixel: VLOADBIAS (hereafter VLOAD), VBIAS1 (hereafter VBIAS), VCOLBIAS (hereafter VCOL), VFLUSH\_LOW (hereafter VFLUSH) and VRESET1\_LOW (hereafter VRESET). The first three of these voltages are part of the output chain of the sensor, which Fig. 23 below shows.

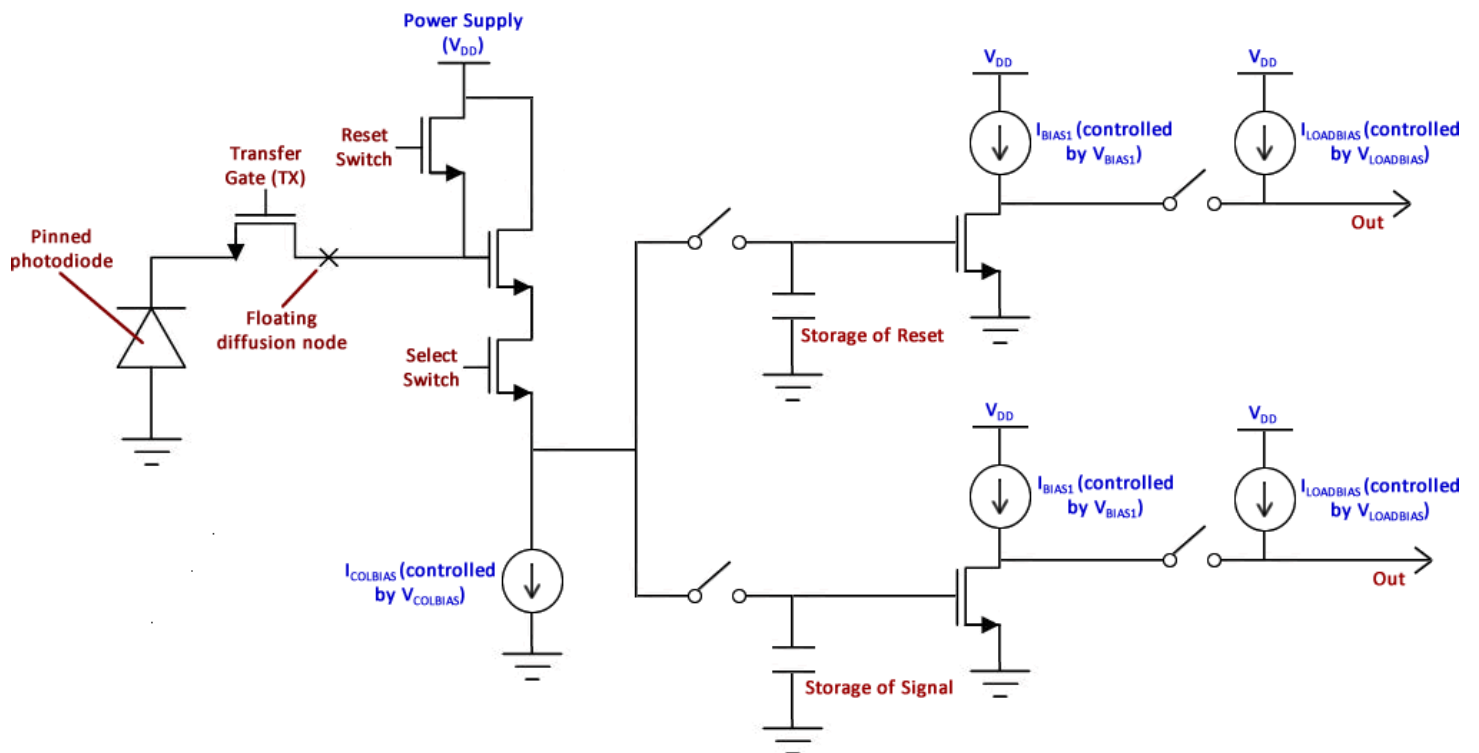


Fig. 23 – FORTIS pixel and output chain (adapted from <sup>[6]</sup>)

The two output chains are identical except that the upper one stores the reset value and the lower one stores the signal value. All three of these voltages affect both the reset and signal outputs. VRESET1 and VFLUSH are reference voltages for the reset and signal lines during the amplifying output chain. These two reference voltages had a large effect on both dynamic range and noise. This is particularly true for FORTIS because of its high conversion gain – if the reference voltages are set incorrectly, the output chain can saturate. It was discovered that if

they were too low, noise was increased. If they were too close together or too far apart, the slope of the log-log PTC became non-linear, producing unreliable results.

Intensity sweeps were used to calculate the noise once it was thought that the voltages were optimised. If the noise was higher than expected, the two reference voltages were tweaked until the lowest noise result was obtained. The other three voltages did not significantly affect noise.

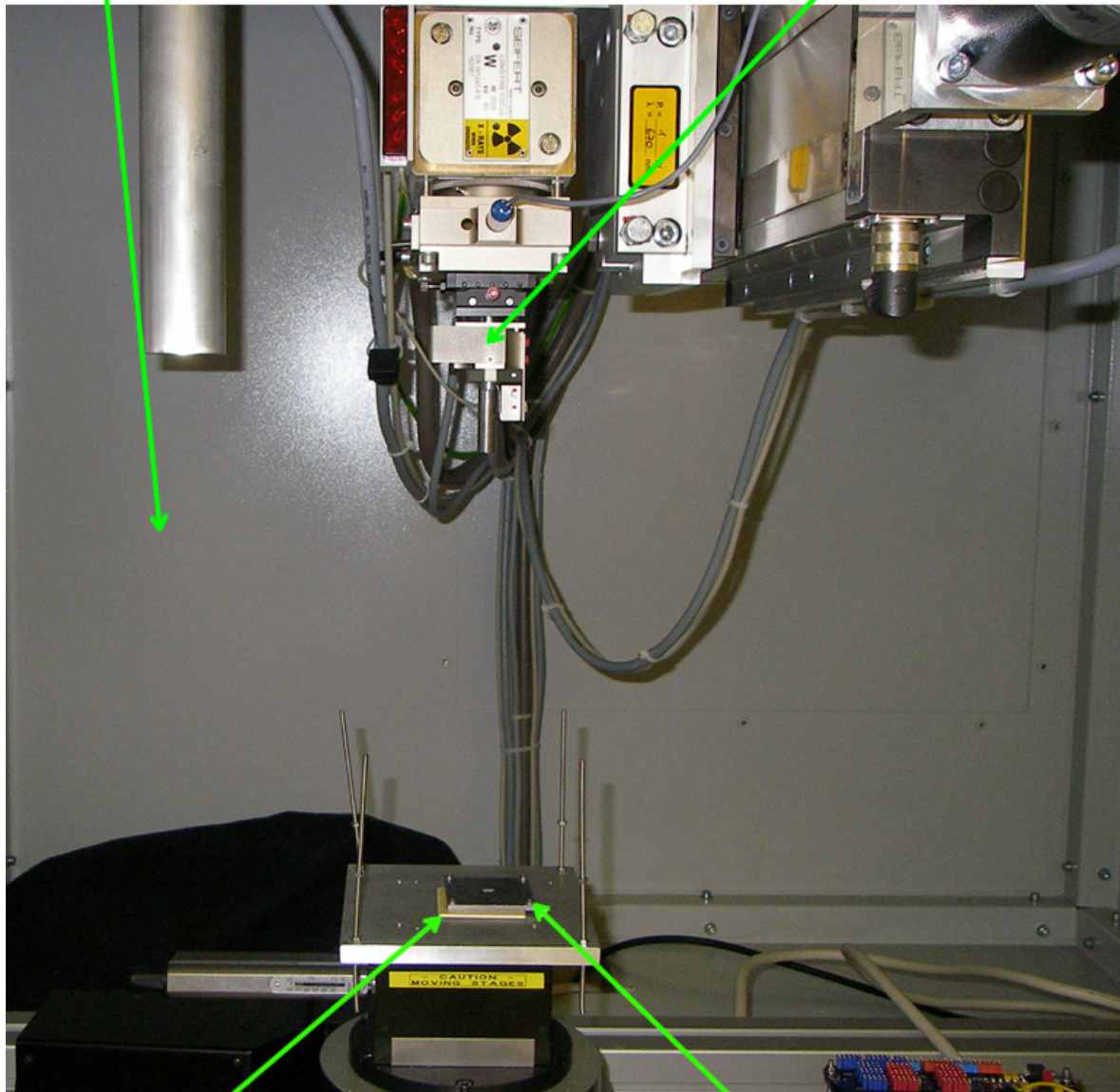
### **(3.2c) Radiation Hardness**

FORTIS 1.0 was chosen to undergo *radiation hardness* testing. This involves exposing the sensor to electromagnetic radiation in various dosage steps and retesting in order to discover how resistant the sensor is to radiation damage. Radiation damage can have many undesirable effects on a sensor and can, with high enough dosages, render it completely useless (see *Section 2.4*). *Fig. 24* below is an annotated photo showing the irradiation setup used for this experiment.



Irradiation Chamber

X-Ray Generator (height adjustable)



Sensor (not shown)

Lead Shield

**Fig. 24 – Irradiation setup**

The first step of the test process involved optimising and characterising five different chips from processing variation 2 (which would theoretically be the best performing processing variation), named RAD1-RAD5, using the same method as before (see *Section 3.2b*). Each sensor was then assigned particular tests (see *Table 1* below) in order to discover if and how various properties

would change due to radiation damage. A lead shield was used to protect the rest of the chip from radiation damage. A small hole allowed a portion of the pixel being tested (later chosen to be B2) to be exposed to the x-rays. The irradiation exposure was accomplished using a 50kV X-ray tube with a 4cm diameter beam, giving a dose rate of 720Gy per hour.

| Sensor:         |         | RAD1      |   |             | RAD2      |   |   |           |   |   | RAD3        |           | RAD4      |           | RAD5      |   |   |
|-----------------|---------|-----------|---|-------------|-----------|---|---|-----------|---|---|-------------|-----------|-----------|-----------|-----------|---|---|
| Sweep Type:     |         | Intensity |   | Integration | Intensity |   |   | Annealing |   |   | Integration | Image Lag | Intensity | Image Lag | Intensity |   |   |
| Level           | Colour: | R         | B | G           | R         | B | G | R         | G | B | G           | G         | G         | G         | R         | G | B |
| Pre-Irradiation |         |           |   |             |           |   |   |           |   |   |             |           |           |           |           |   |   |
| 0.02 kGy        |         |           |   |             |           |   |   |           |   |   |             |           |           |           |           |   |   |
| 0.04 kGy        |         |           |   |             |           |   |   |           |   |   |             |           |           |           |           |   |   |
| 0.11 kGy        |         |           |   |             |           |   |   |           |   |   |             |           |           |           |           |   |   |
| 0.22 kGy        |         |           |   |             |           |   |   |           |   |   |             |           |           |           |           |   |   |
| 0.44 kGy        |         |           |   |             |           |   |   |           |   |   |             |           |           |           |           |   |   |
| 1.11 kGy        |         |           |   |             |           |   |   |           |   |   |             |           |           |           |           |   |   |
| 1.33 kGy        |         |           |   |             |           |   |   |           |   |   |             |           |           |           |           |   |   |
| 1.56 kGy        |         |           |   |             |           |   |   |           |   |   |             |           |           |           |           |   |   |
| 1.78 kGy        |         |           |   |             |           |   |   |           |   |   |             |           |           |           |           |   |   |
| 2.00 kGy        |         |           |   |             |           |   |   |           |   |   |             |           |           |           |           |   |   |
| 2.22 kGy        |         |           |   |             |           |   |   |           |   |   |             |           |           |           |           |   |   |

KEY: Green = tested, Grey = not tested, Red = tested but data cannot produce results.

Table 1 – FORTIS 1.0 radiation hardness test plan

Each of the sensors was then scheduled to be exposed to a certain amount of radiation (initially 0.02 kGy) and retested using the same conditions as before in order to determine the effects of the radiation exposure. This process continued for each level of radiation exposure for all five sensors. When the sensors were not being exposed to radiation or tested, they were kept in a freezer at approximately -25°C in order to prevent annealing in between each radiation exposure.

An additional test was planned in order to develop an annealing profile for a single chip. The reason for this was to discover how long it took for the sensor to recover to normal operation

after radiation exposure. RAD2 was chosen for this test. After its final exposure at 2.22 kGy, it would be tested as usual and then retested numerous times throughout the rest of the week without it being returned to the freezer.

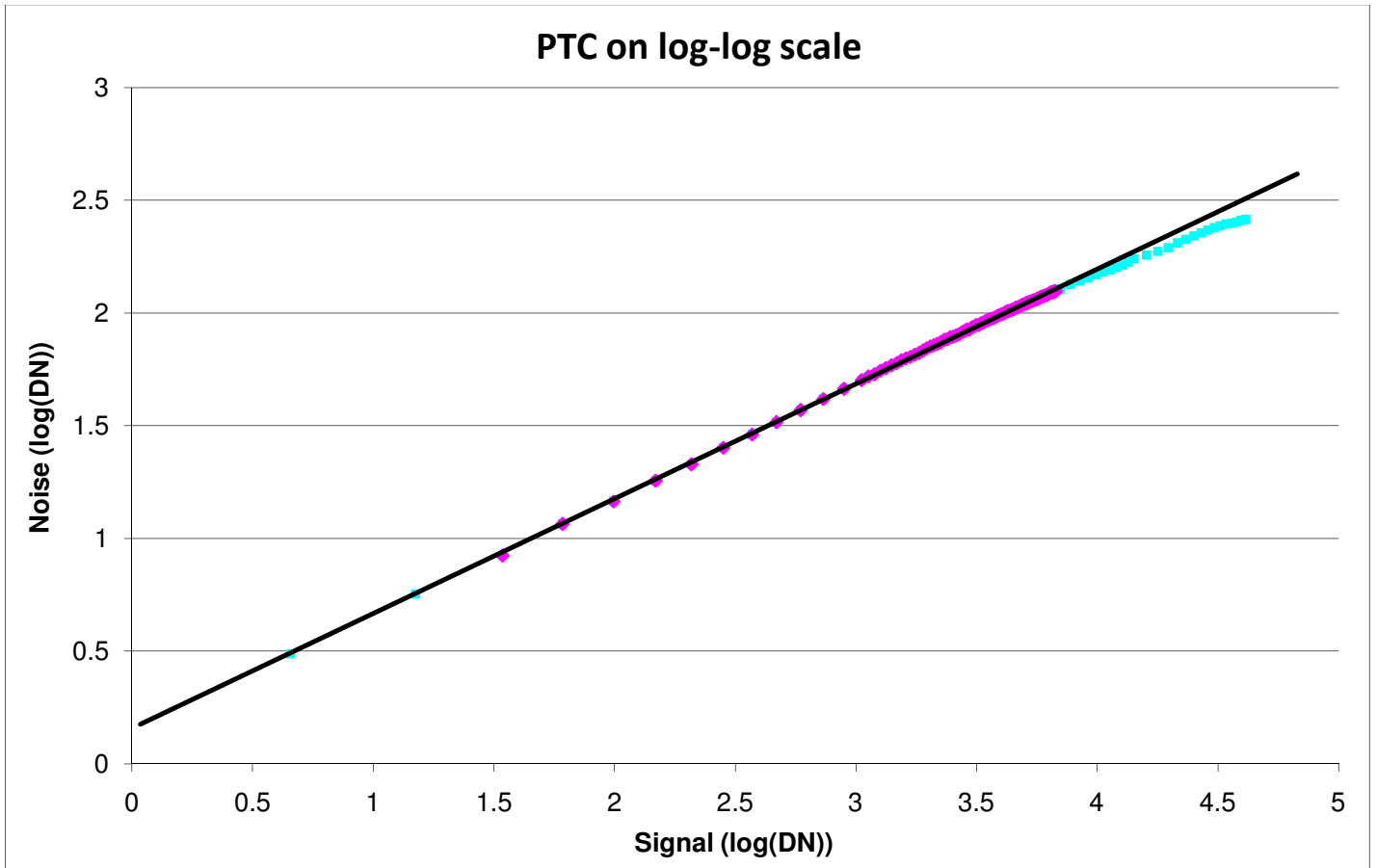
### **(3.3) TAKING AND ANALYSING RESULTS**

Three FORTIS 1.0 pixels were available for testing: A2, B2 and C2. All three of these pixels on all three processing variations were optimised and characterised using intensity sweeps. Dark current was not measured.

Once intensity sweep results were obtained, they were investigated using a *per pixel analysis* method. This was done using a custom-made LabVIEW program which calculates several properties of each pixel (the most important of which being the mean signal at a given intensity and the variance in this mean signal) and outputs an average PTC, as well as other information such as photon counts, to a spreadsheet. From there, a log-log PTC is created with a line of best fit. The boundaries of this best fit line are adjusted until they produce a gradient as close as possible to 0.5 (being careful to choose a range of points that appear sufficiently linear) in order to work out the average shot noise of the sensor. This best fit line also provides us with a value for the gain and quantum efficiency, and a value for full well capacity can be obtained from the peak value on the PTC. Combining this with the gain and photon count, this tells us the maximum number of photons that can be detected as well as the maximum number of electrons released.

*Fig. 25* shows such a spreadsheet that has been analysed to produce good results. *Fig. 26* shows results that do not provide sufficient results – the log-log PTC graph is quite obviously

erroneous. In this case, the cause of this non-linearity was our reference voltages being too close together.



**Fig. 25** – Good results based on log-log PTC showing linearity in the shot noise (highlighted pink) section, with a gradient 0.5

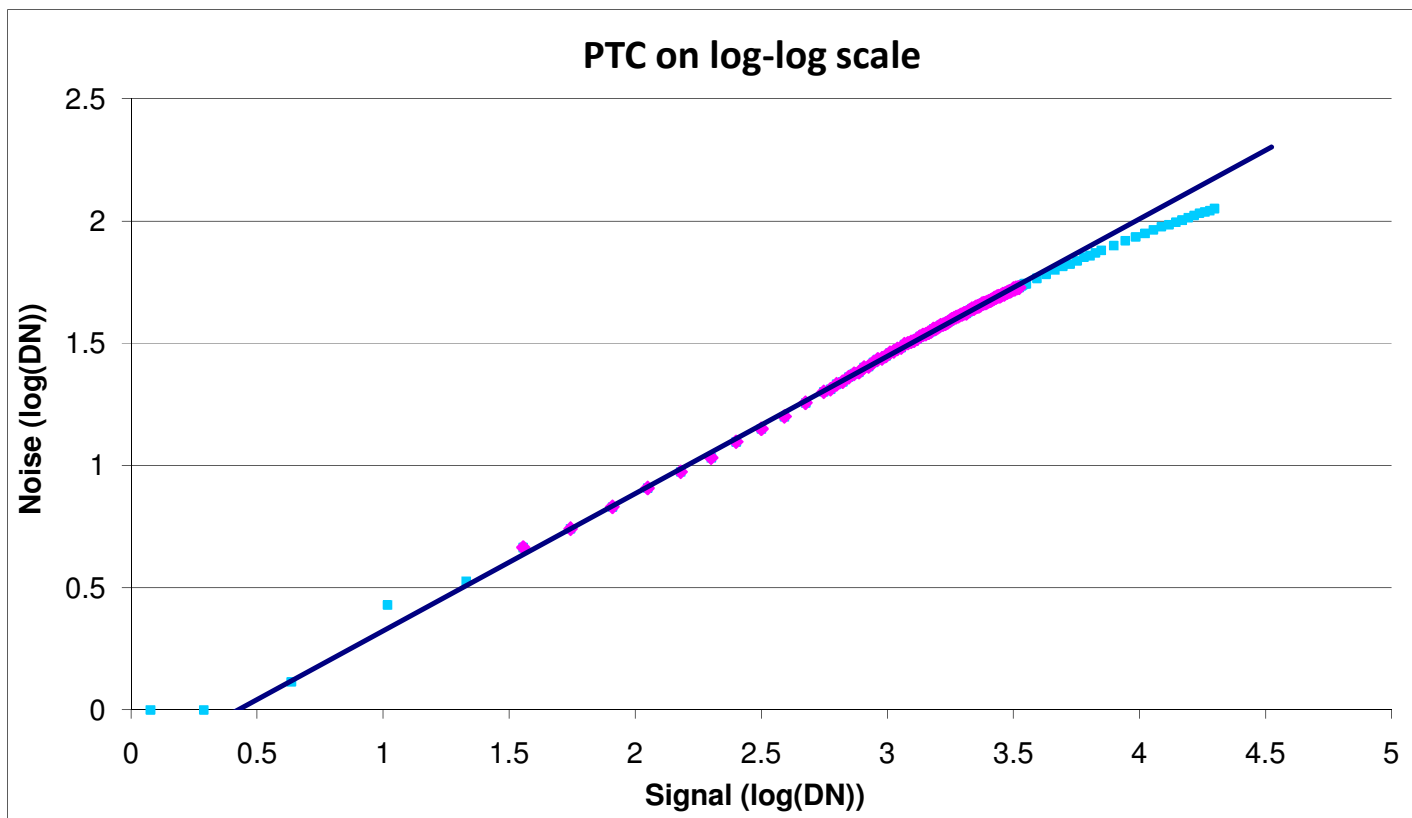


Fig. 26 – Results based on log-log PTC showing non-linearity (gradient of pink section is 0.56)

### (3.3a) Software Development (Per Pixel Analysis)

A significant portion of my time during the placement was devoted to creating LabVIEW programs. Several small programs were written as part of the aSpect upgrade performed to *tester 1* in May 2009. The new system is designed to allow switching between operation modes by simply changing a single option, rather than having to move files around and alter various parameters in a spreadsheet. It also makes it far easier to recreate or modify previously made vectors (because their source pattern sheets are kept with them) and it is also possible to store and automatically apply certain settings such as clock speed, frame size and which scripts to use for intensity and integration sweeps.

The main LabVIEW project I was tasked with was a new version of the *per pixel analysis* software that is used to calculate sensor properties based on sweep data. The new program is no longer linear in its operation and the main improvements are:

- Significantly lower disk space usage. This is achieved by programming idVIEW to create mean and variance images from a set of raw frames rather than doing so on the fly in the analysis stage.
- Significantly faster loading times due to fewer files having to be read, plus optimised code.
- The ability to view each average and variance frame individually on-screen.
- Easier to use and more flexible region of interest selection. This is achieved by allowing the user to graphically draw a rectangle over a preview image rather than entering numbers in text boxes.
- The ability to recalculate results when changing properties such as the region of interest without having to re-read each file.
- The ability to set a minimum  $R^2$  value for the linear section of each pixel's PTC. Any pixels below this threshold are marked and counted so that the user can see a measure of how many pixels produce acceptable PTCs.
- The creation of histograms for various sensor properties, as well as the display of live signal and noise histograms within the program.
- The ability to view and interpret a log-log average PTC graph to get overall results for noise, gain and quantum efficiency and directly.

- The number of parameters that the user must specify before running the program is reduced because properties such as the number of frames per intensity are detected automatically.
- Sequence integration. Once a sweep is completed, the per pixel analysis program opens and imports the just-captured data automatically without the user having to launch the program and specify the data location manually.
- The addition of FPN, DSNU and PRNU calculations.

The program was completed in September 2009 and received a few updates since then to tweak the GUI, add extra features (such as additional output data, value indicators and graphs and a new dark current calculation method) and fix minor bugs. It was used to analyse the data captured in FORTIS 1.0's radiation hardness tests and FORTIS 1.1 results. The program will continue to be used at RAL, including for FORTIS 1.1's radiation hardness testing.

Along with the main program, several related programs were created, labelled "Per Pixel Analysis tools" that used modified subroutines from the main program to perform related tasks. The first of these tools is a program that allows for the conversion of older raw frame data into the mean and variance images that are required by the new Per Pixel Analysis program. Other programs perform tasks such as displaying an image (including 16-bit signed/unsigned images that cannot be read by most imaging programs), comparing two images by switching between them on-the-fly and subtracting one from the other, and cropping an entire set of image data automatically. Screenshots of the programs mentioned in this section can be seen in *Appendix C*.

## (4) RESULTS

Table 3 in Appendix A provides a summary of the differences between the three pixel structures, A2, B2 and C2, mentioned throughout this section.

### (4.1) FORTIS 1.0 OPTIMISATION RESULTS

Fig. 27 shows the timing optimisation results for the A2 pixel on processing variation 1 (chip 1). All of the sensors on all of the processing variations that were characterised showed similar results and almost all of them produced the best dynamic range using the same timings (one or two only differing by  $1\mu\text{s}$  on a single signal).

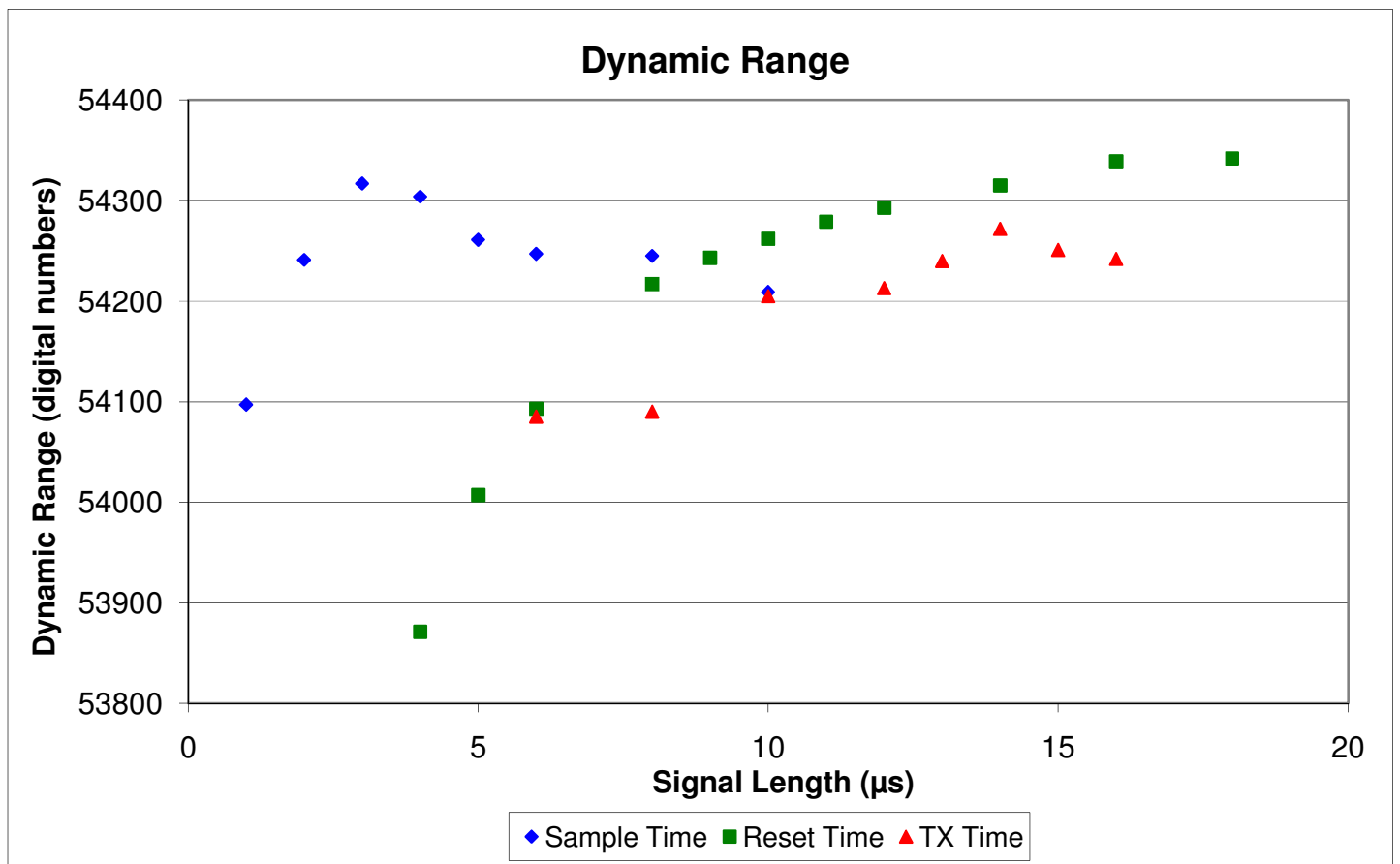


Fig. 27 – Timing optimisation for pixel A2 on split 1



Fig. 28 shows later measurements that were taken on pixel B2 in order to determine whether the short 1 $\mu$ s gaps between both the Reset and Sample R and the TX and Sample S signals supplied the best dynamic range. It is clear that shorter gaps are the optimum solution, so they were kept at 1 $\mu$ s.

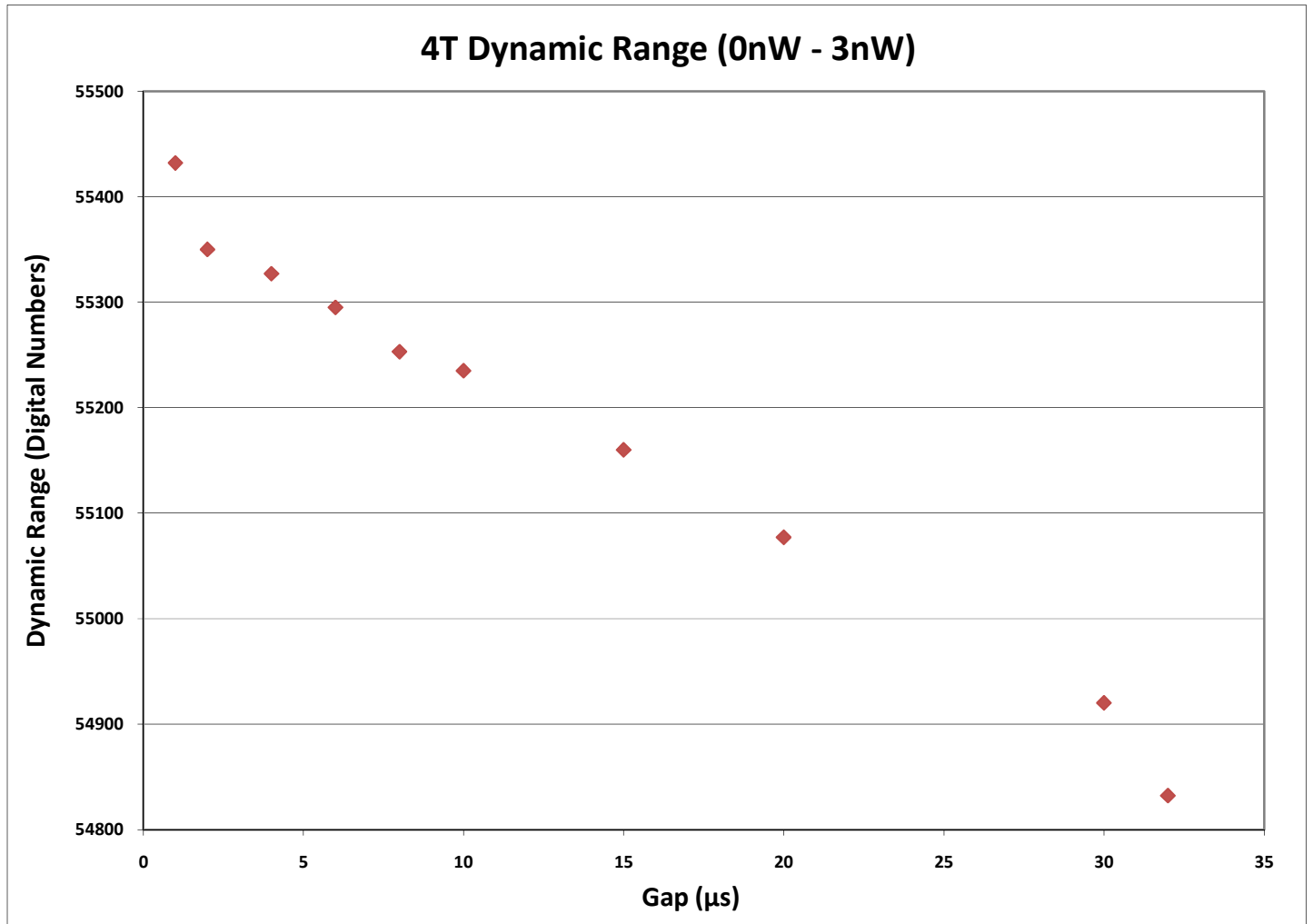
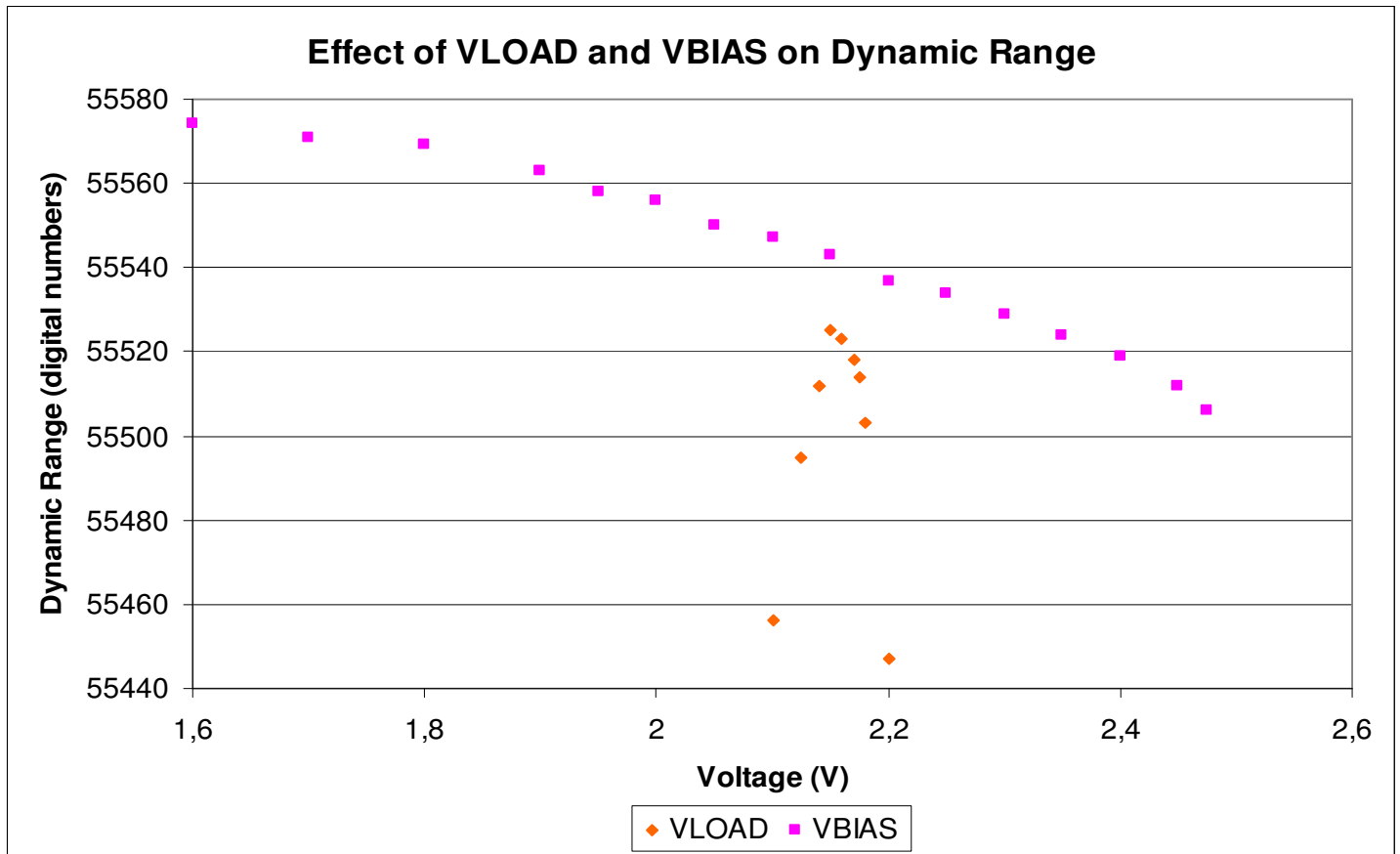


Fig. 28 – Timing optimisation for pixel B2 on split 1

Voltage optimisations did not prove to be as consistent. Even different chips within the same processing variation required different voltages for the same pixel type. However, the differences were small enough that an average optimal voltage setting could be applied to all of

them to give the best results. *Figs. 29-31* show voltage optimisation results for the B2 pixel on a chip from processing variation 2.



*Fig. 29 – VLOAD and VBIAS optimisation for pixel B2 on a split 2 sensor*

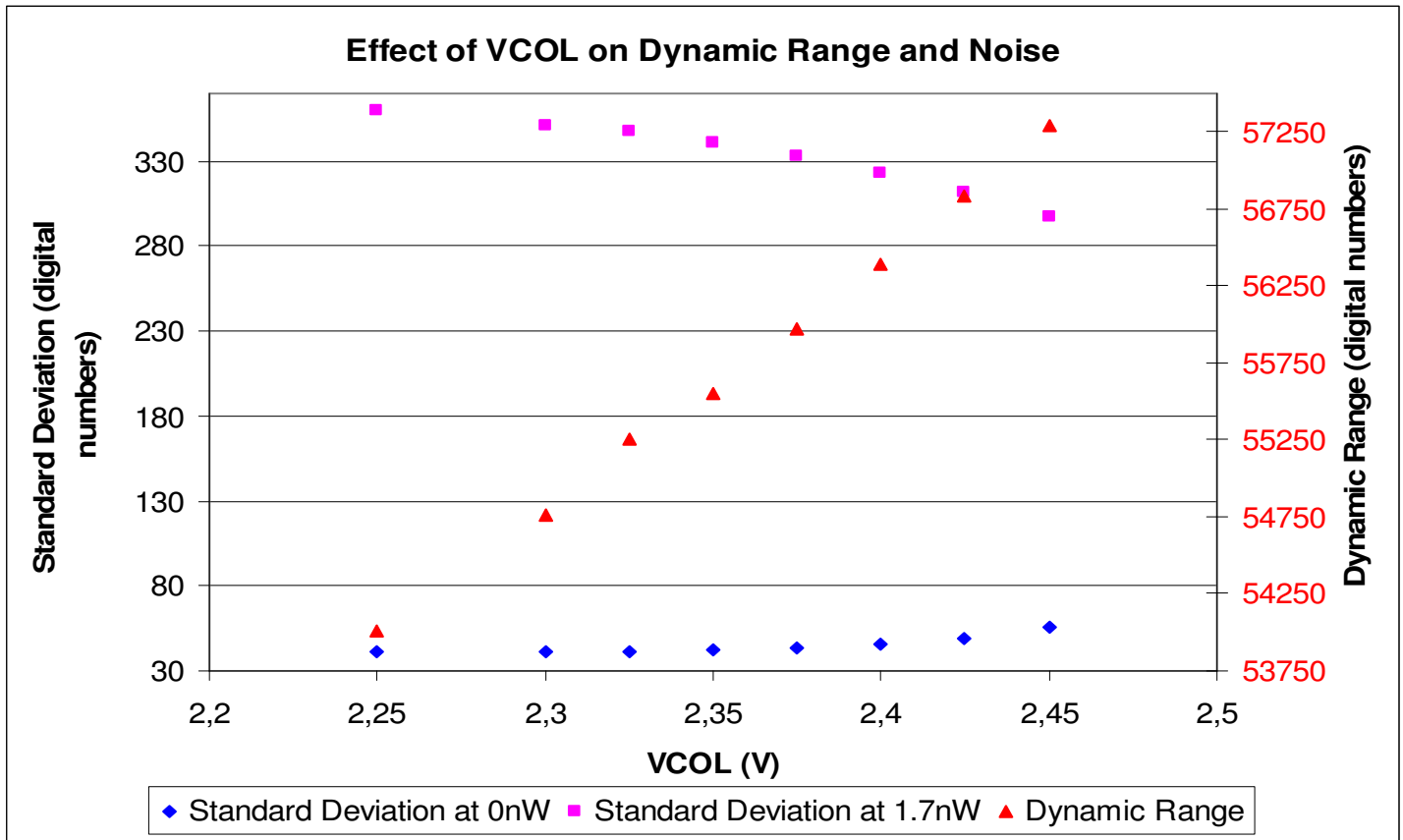
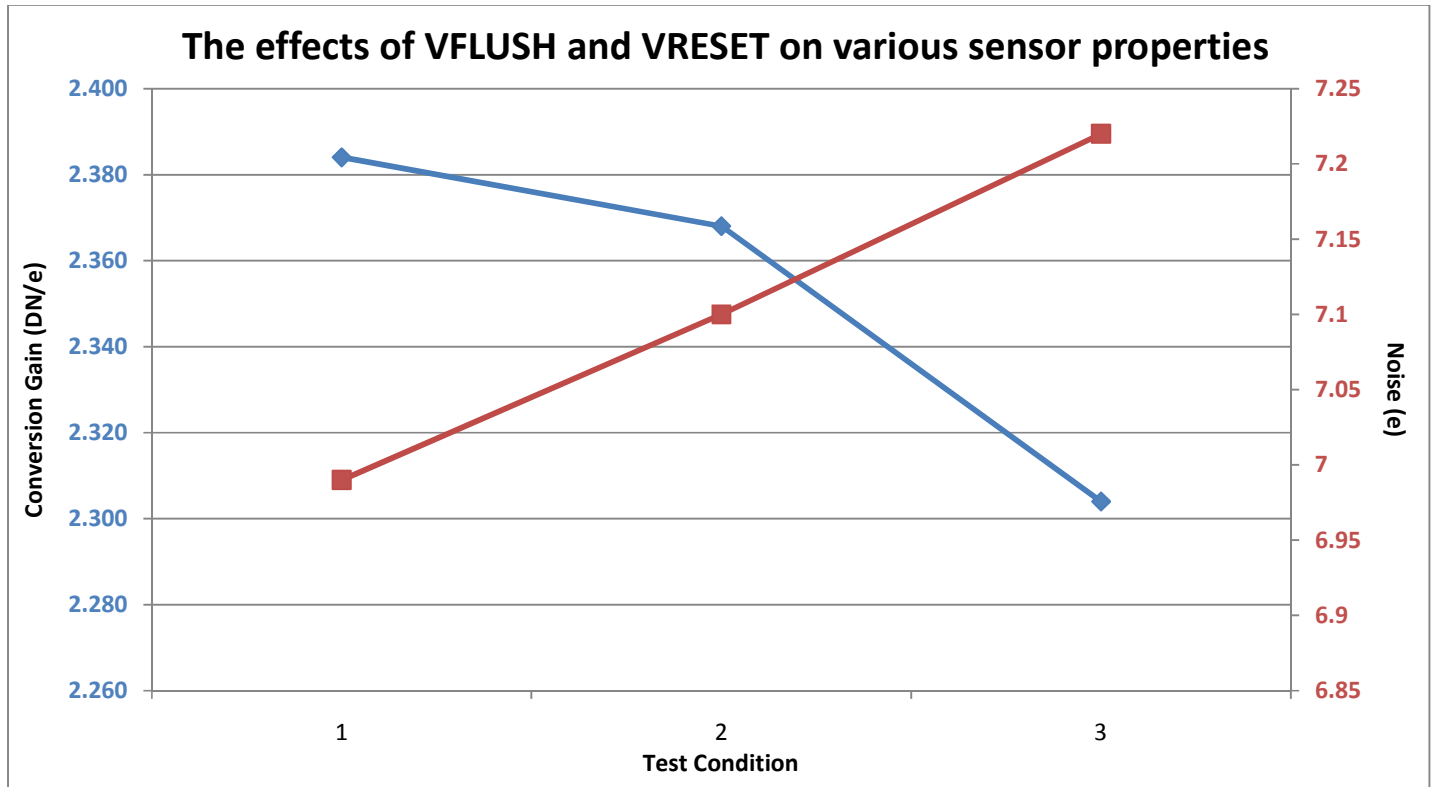


Fig. 30 – VCOL optimisation for pixel B2 on a split 2 sensor

As can be seen from Fig. 30, the optimum setting for VCOL would have to be a compromise. It was expected that the higher the current (and so the lower the voltage), the lower the noise. However, the circuitry responds too quickly with higher current, which limits dynamic range. Because, in most applications, noise at low light levels is more important than noise at high light intensities, the value of 2.4V was chosen in this case as providing the highest dynamic range and lowest high light intensity noise before the low light intensity noise started noticeably increasing.

Lastly, Fig. 31 shows the results obtained with various combinations of VRESET1\_LOW and VFLUSH\_LOW voltages.



| Test Condition | VFLUSH_LOW | VRESET_LOW |
|----------------|------------|------------|
| 1              | 1.38       | 1.29       |
| 2              | 1.4        | 1.3        |
| 3              | 1.4        | 1.31       |

**Fig. 31** – Reference voltage optimisation for pixel B2 on a split 2 sensor (square = noise, diamond = conversion gain)

It is clear that test condition 1 (VFLUSH\_LOW at 1.38V, VRESET1\_LOW at 1.29V) provides the best results in this case – both highest conversion gain and lowest noise. *Tables 4-6 in Appendix B* summarise the final optimised timings and voltages for the initial test chips on all three processing variations. The best chips from each processing variation were chosen for these tests.

## (4.2) FORTIS 1.0 FINAL RESULTS

Table 2 below shows the results obtained from intensity sweeps after timing and voltage optimisation of each pixel on each processing variation. Figs. 32-35 show graphical representations of the gain, quantum efficiency and noise results from this table.

| Pixel     | Gain (DN/e)<br>±0.02 | QE (%)<br>±0.2 | Noise (e)<br>±0.5 | Linear Full Well<br>±300 | Maximum Full Well<br>±400 |
|-----------|----------------------|----------------|-------------------|--------------------------|---------------------------|
| S3C1 - C2 | 1.67                 | 32.8           | 11.6              | 21547                    | 32065                     |
| S2C3 - C2 | 1.73                 | 30.2           | 10.5              | 24291                    | 17179                     |
| S1C2 - C2 | 1.68                 | 32.6           | 10.2              | 23486                    | 30053                     |
| S3C1 - B2 | 2.33                 | 30.8           | 6.5               | 19701                    | 17566                     |
| S2C3 - B2 | 2.41                 | 30.0           | 6.0               | 19114                    | 23340                     |
| S1C2 - B2 | 2.36                 | 32.2           | 6.1               | 18728                    | 23420                     |
| S3C1 - A2 | 0.86                 | 9.9            | 19.2              | 46090                    | 63902                     |
| S2C3 - A2 | 0.66                 | 12.6           | 22.2              | 63443                    | 75060                     |
| S1C2 - A2 | 0.66                 | 12.9           | 20.0              | 39414                    | 54256                     |

Table 2 – Results for initial test chips

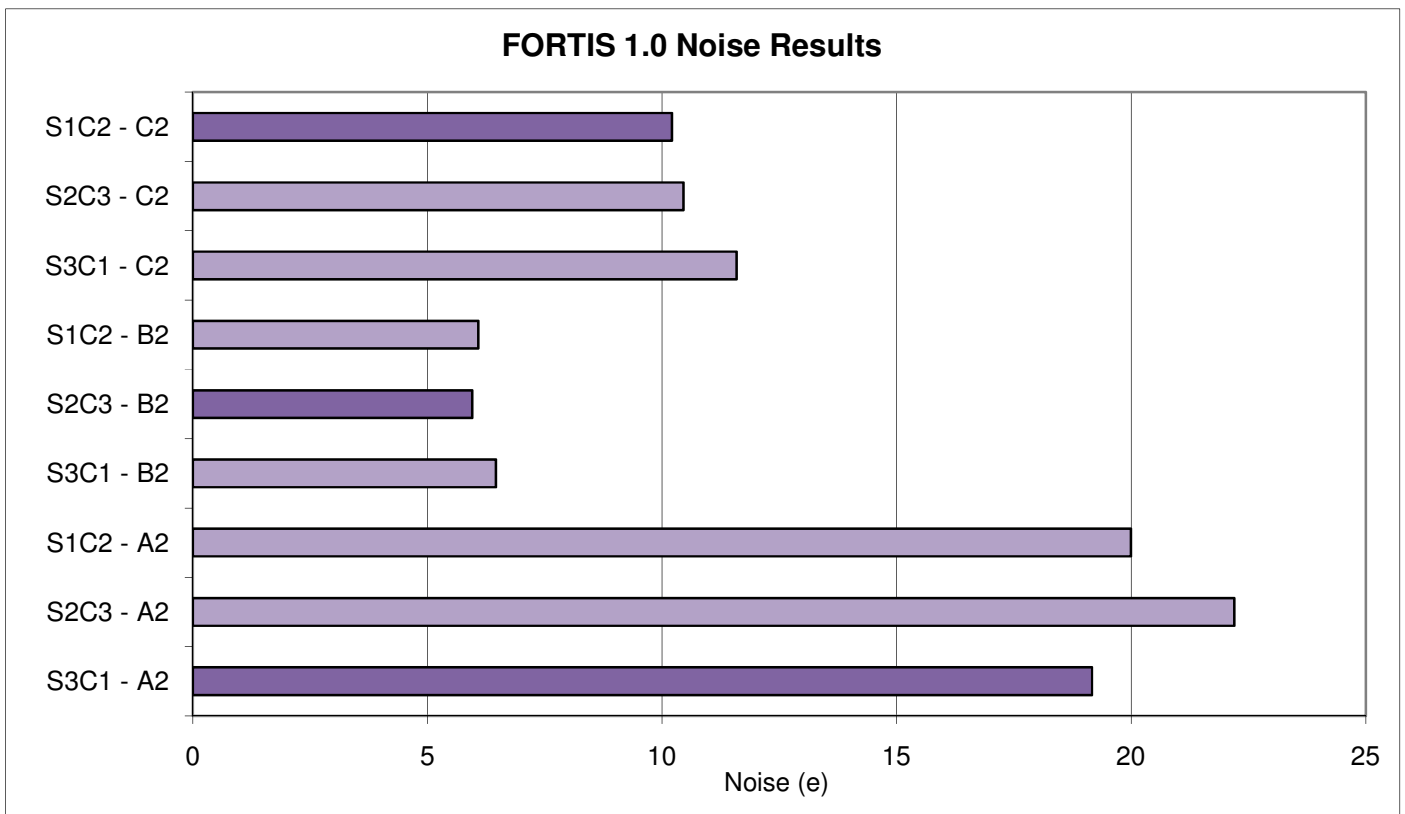
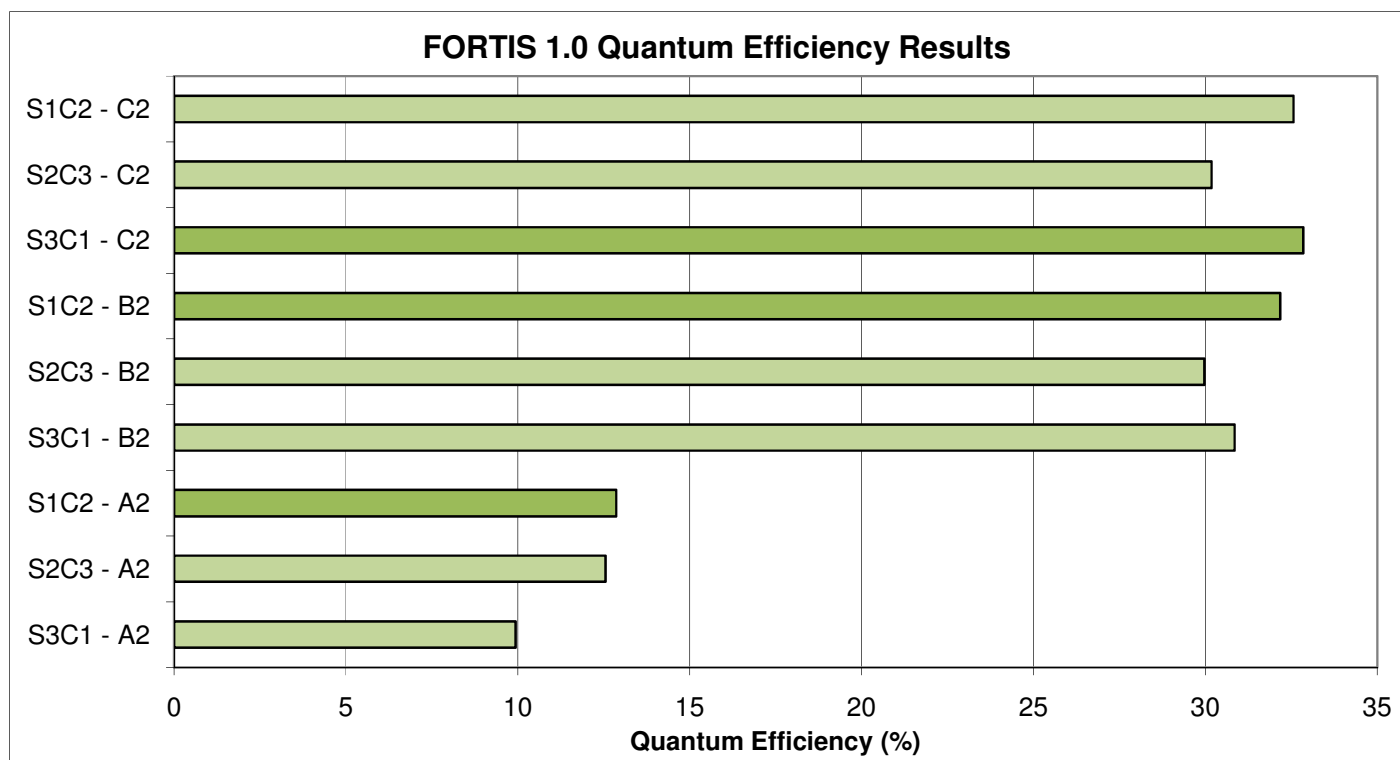
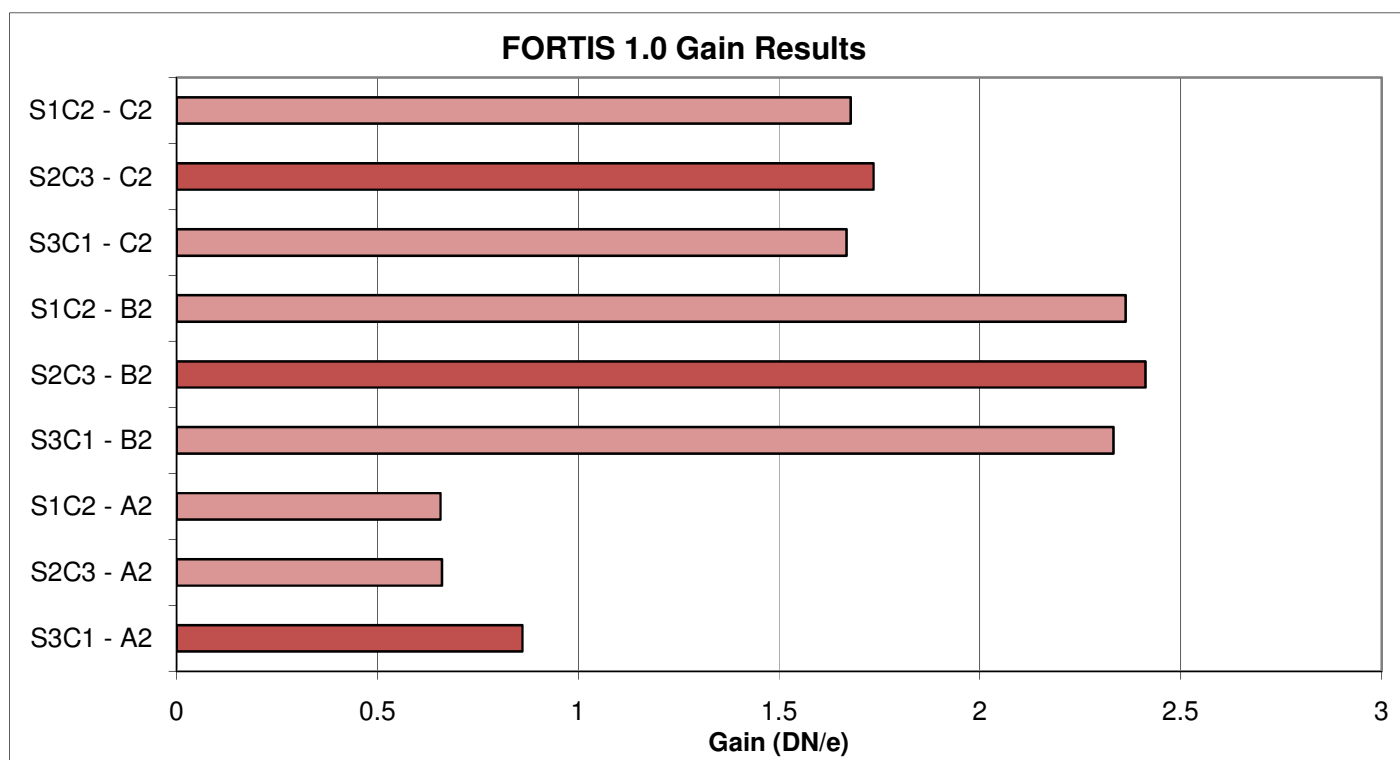


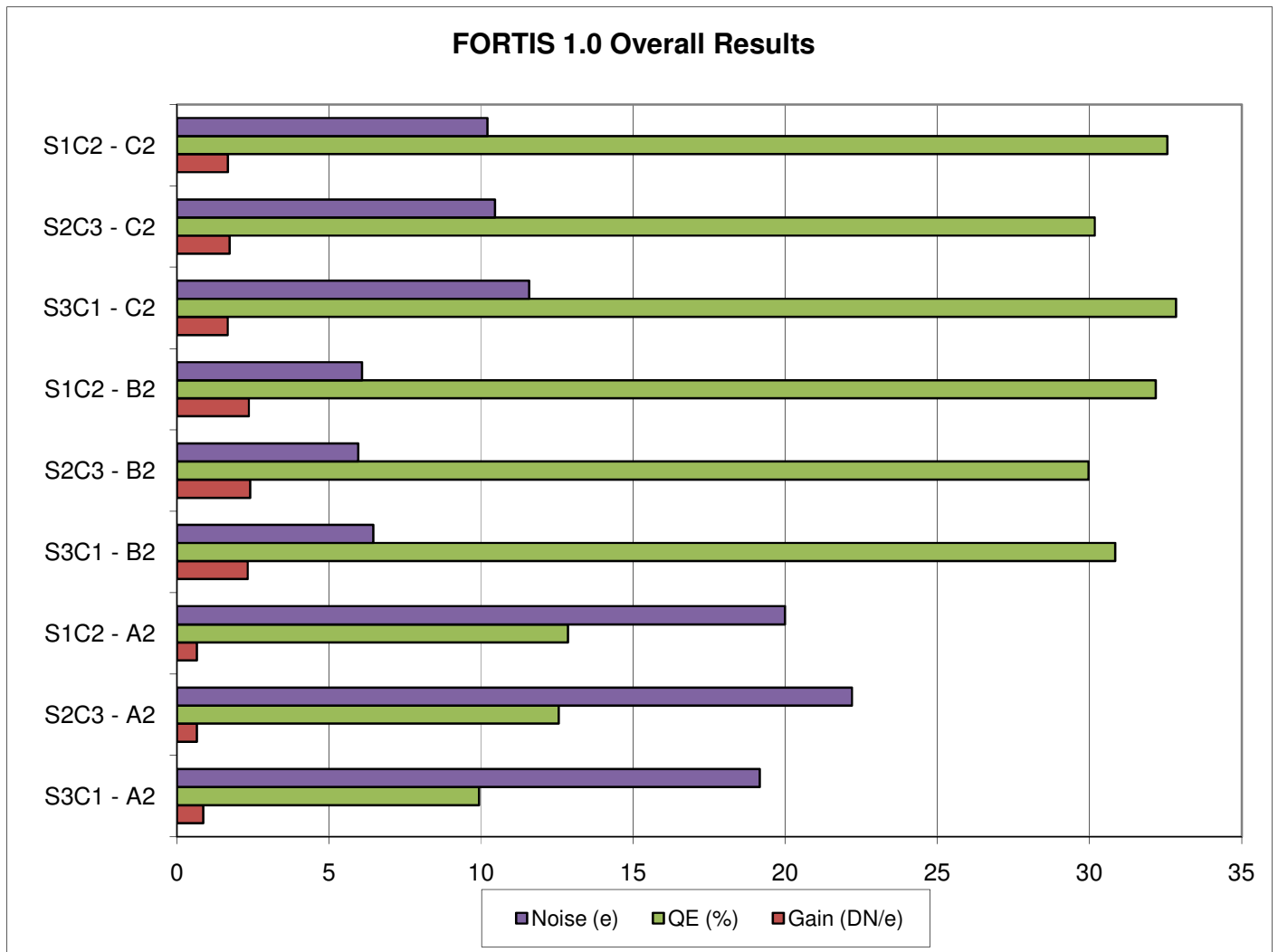
Fig. 32 – Noise results for FORTIS 1.0



**Fig. 33** – Quantum Efficiency results for FORTIS 1.0



**Fig. 34** – Gain results for FORTIS 1.0



*Fig. 35 – Summary results for initial test chips*

The first immediately obvious detail this graph shows is the inferior performance of the A2 pixel (the control 15 $\mu$ m pixel). Not only does it have the highest noise (161% higher than the average of B2 and C2) of all three pixels but also the lowest gain (57% lower than the average of B2 and C2) and quantum efficiency (62% lower than the average of B2 and C2). This high noise and low gain was expected due to its higher floating diffusion node capacitance. However, the lower quantum efficiency is suspicious. The B2 pixel (with the L-shaped active area) has the lowest noise of all three pixel types, averaging 6.17e between the three processing variations. The C2

pixel (with its differently sized and shaped source follower) was, in theory, supposed to have reduced random telegraph noise but the effect on other noise sources may have been detrimental, leading to the results seen here. It was agreed that the error in our noise results was approximately  $\pm 0.5e$  due to the general change in results we found when testing numerous times under the same conditions.

This B2 pixel is the lowest noise pixel ever created by the CMOS Image Sensor group at RAL. In fact, early characterisation of another batch of sensors from the ones tested here (now used as *radiation hardness chips*, see *Section 4.3a* for more details) showed a noise level of often slightly lower than  $6e$ , with the lowest recorded value being  $5.7e$  (produced by RAD4, from processing variation 2). In terms of processing variations, it appears that the control processing variation (1) produces the best noise results for pixels B2 and C2 without sacrificing gain or quantum efficiency, whilst the third processing variation (which has an increase in N doping of the diode) produces the worst. However, the difference is not very significant and not consistent among the different chips or sensor performance parameters. It was concluded that the processing variations did not produce any significant measurable differences.

### **(4.3) RADIATION HARDNESS RESULTS**

FORTIS 1.0 was chosen to undergo *radiation hardness* testing. This involved exposing the sensor to electromagnetic radiation in various dosage steps and repeating parameter tests in order to discover how resistant the sensor is to radiation exposure. Because of the superiority of the B2 pixel found in earlier testing (see *Section 4.3*), that pixel type was chosen to undergo these tests. Because the previous FORTIS 1.0 results showed that the different processing variations made



no real difference to the sensors' performance, all five radiation hardness ("rad hard") sensors were from processing variation 2 because we had five sensors from that processing variation ready for use.

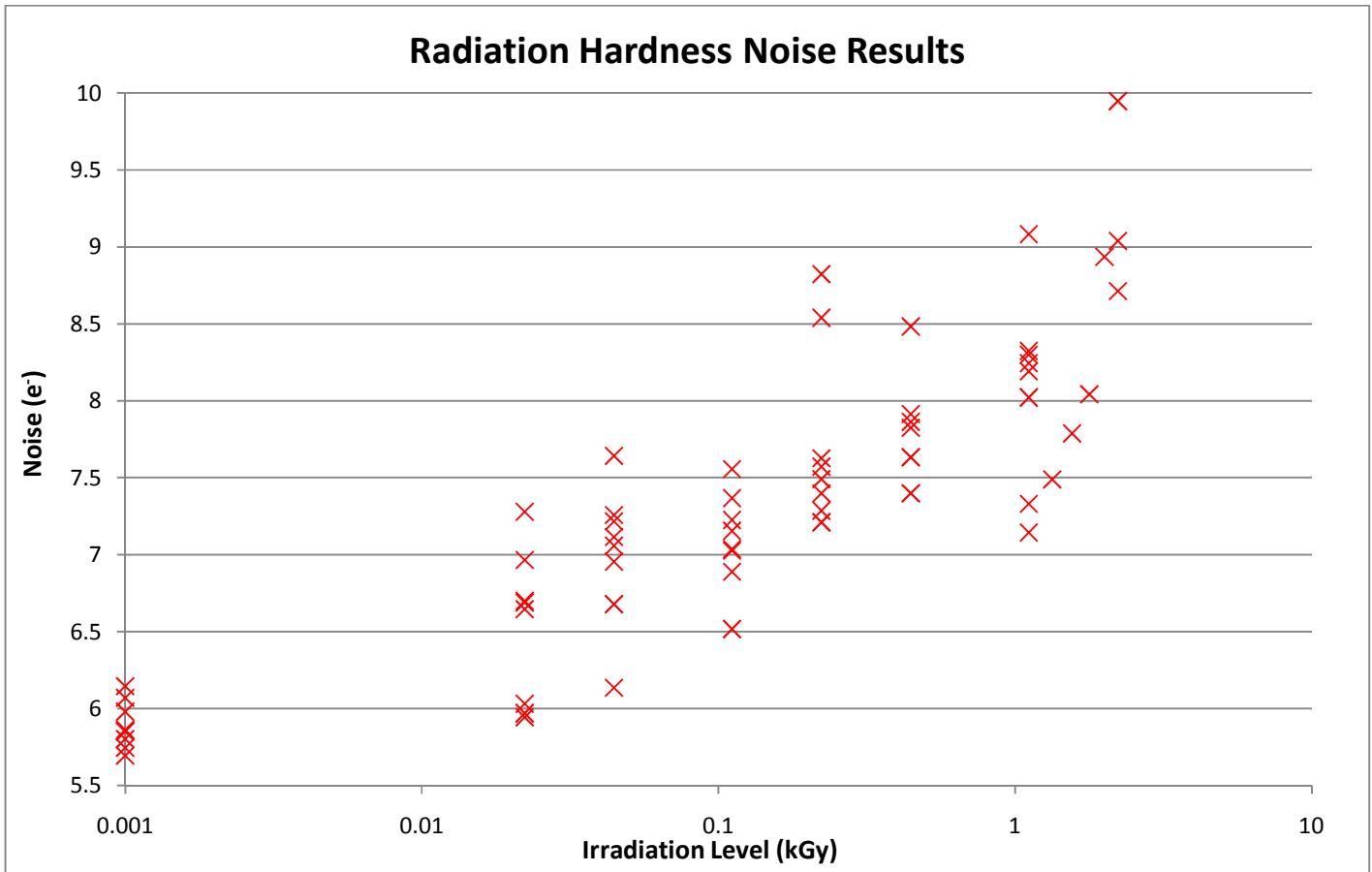
Each of the five sensors was optimised from scratch and their optimised vector timings were averaged. These average vectors were used for all five sensors during all radiation hardness tests to ensure that the vector timings did not have an impact on the results of each sensor. The results of this optimisation process are shown in *Table 7* in *Appendix B*.

The lead shield was designed so that half of the B2 pixel was covered and the other half was not, in order to provide an immediate control, as well as testing the effectiveness of the shield. All of the results were then calculated over a 32x32 area of the exposed portion of the pixel array, totalling 1024 pixels.

Note that all of the graphs in this section have a logarithmic x-axis. Because 0 cannot appear on a logarithmic scale, the control results taken before irradiation are listed as 0.001 kGy.

#### **(4.3a) Noise Results**

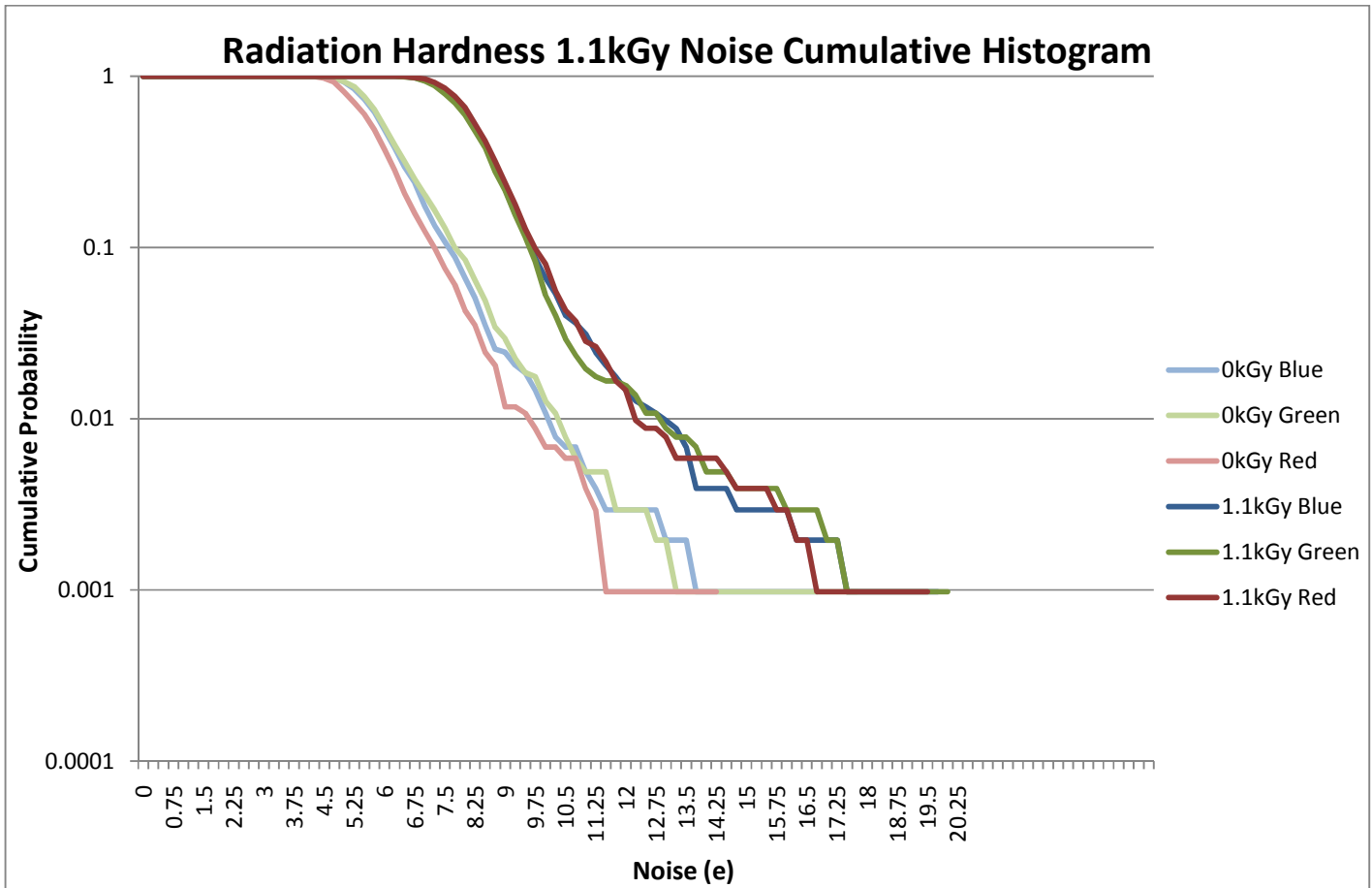
First we will look at the changes to the noise of the exposed area of the pixel array.



**Fig. 36** – Radiation hardness results for noise

Here we see a logarithmic increase in noise with radiation exposure level, which matches previous similar experiments <sup>[12]</sup>. It is also interesting that the variance (or error) in the results seems to increase also – compare the closeness of the graph points from the control test to those from the rest of the exposures. Assuming our noise error of  $\pm 0.5e$ , our results range changes from  $\sim 1.5e$  to  $\sim 2.6e$  by the time we reach 0.11 kGy exposure.

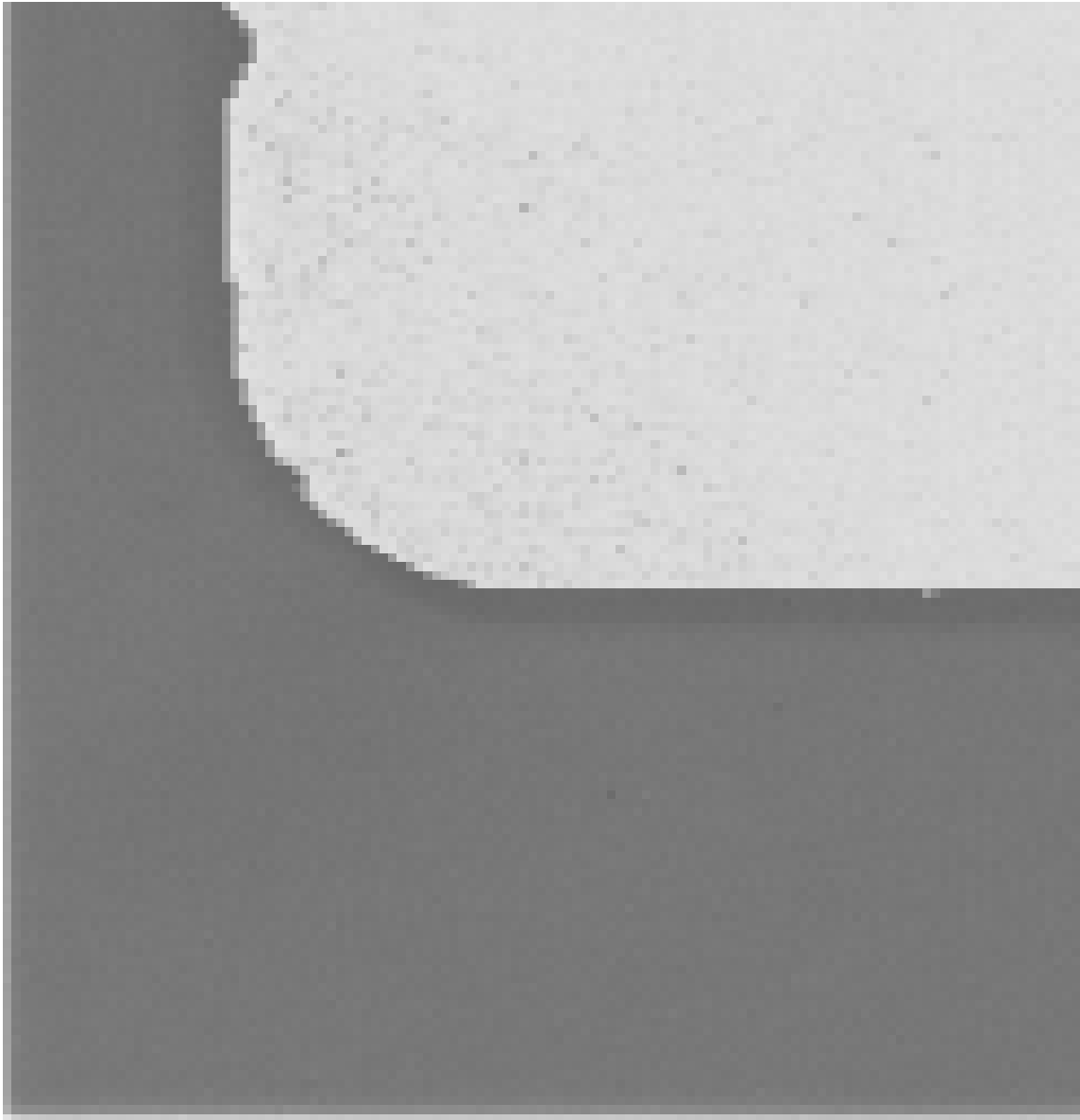
Such an increase in noise is associated with charge trapping in the source follower transistor gate oxide and the corresponding silicon-silicon dioxide interface <sup>[16]</sup>.



**Fig. 37** – Radiation hardness cumulative histogram for noise of a non-irradiated sensor and a 5kGy irradiated sensor

The cumulative histogram shown in Fig. 37 shows the probability of any given pixel to have a noise above the value in the x-axis for each colour and for a pre-irradiated sensor as well as a sensor that has been irradiated to 1.1 kGy. For example, we can see that the probability of a FORTIS 1.0 B2 pixel having a noise greater than 3e, whether irradiated or not, is 1 (100%).

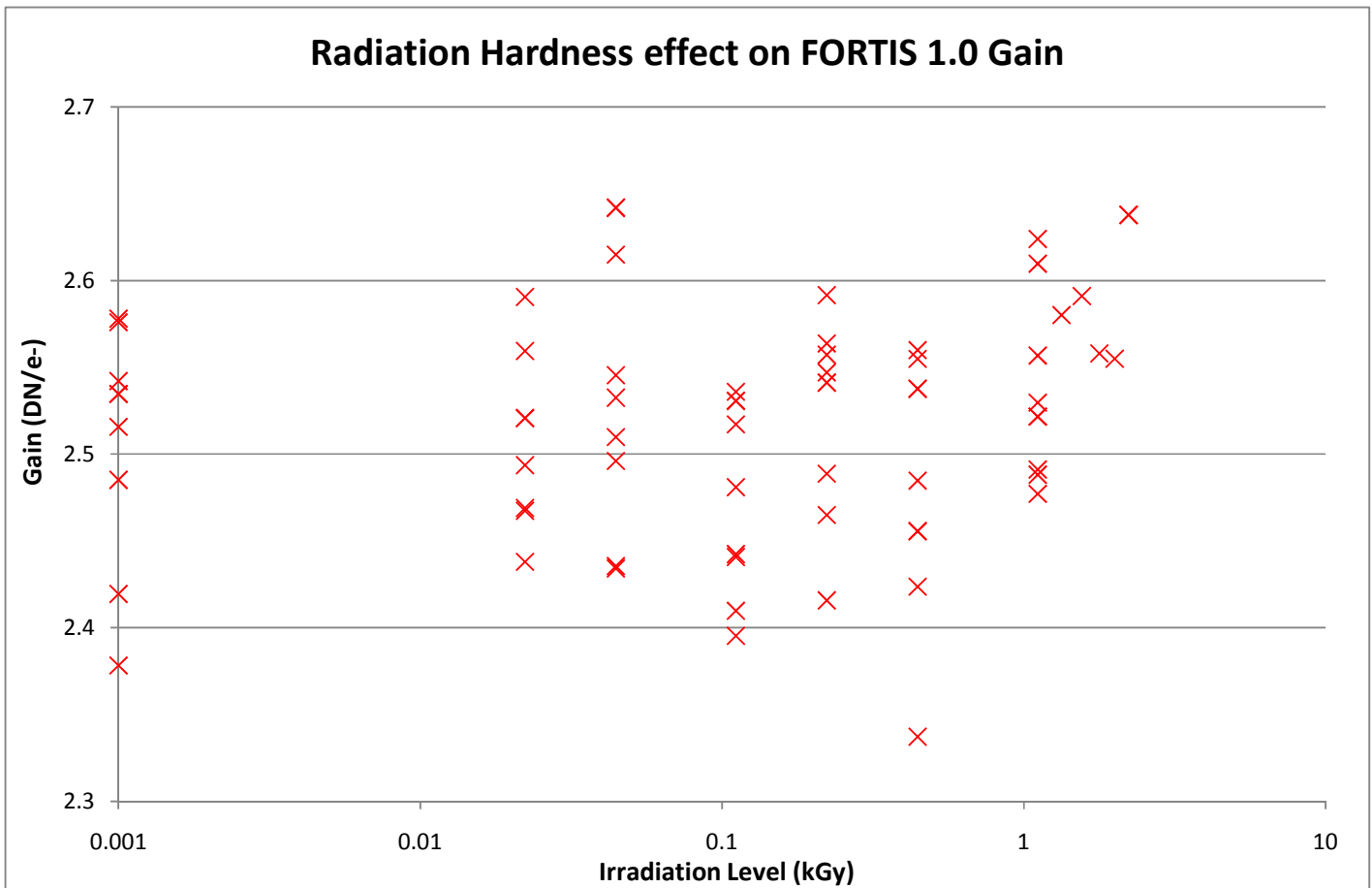
It shows that the histogram for the noise of the pixels doesn't change shape significantly – it merely moves to the right by ~2.5e. The tail of the cumulative histogram is slightly further shifted though, showing a higher probability of unusually high noise pixels. Fig. 38 is a screenshot demonstrating the how this noise change appears in the Per Pixel Analysis program:



**Fig. 38** – Screenshot of Per Pixel Analysis showing an increase in variance (directly related to noise) of the exposed area of the B2 pixel array in the dark

Note how the variance in each pixel's value (taken from 90 frames per light intensity) is split into two distinct sections – the darker, low variance area that was unexposed and the lighter, high variance area damaged by radiation. The shield appears to work very well at preventing the X-rays from damaging the areas of the sensor it was supposed to protect.

#### (4.3b) Conversion Gain Results

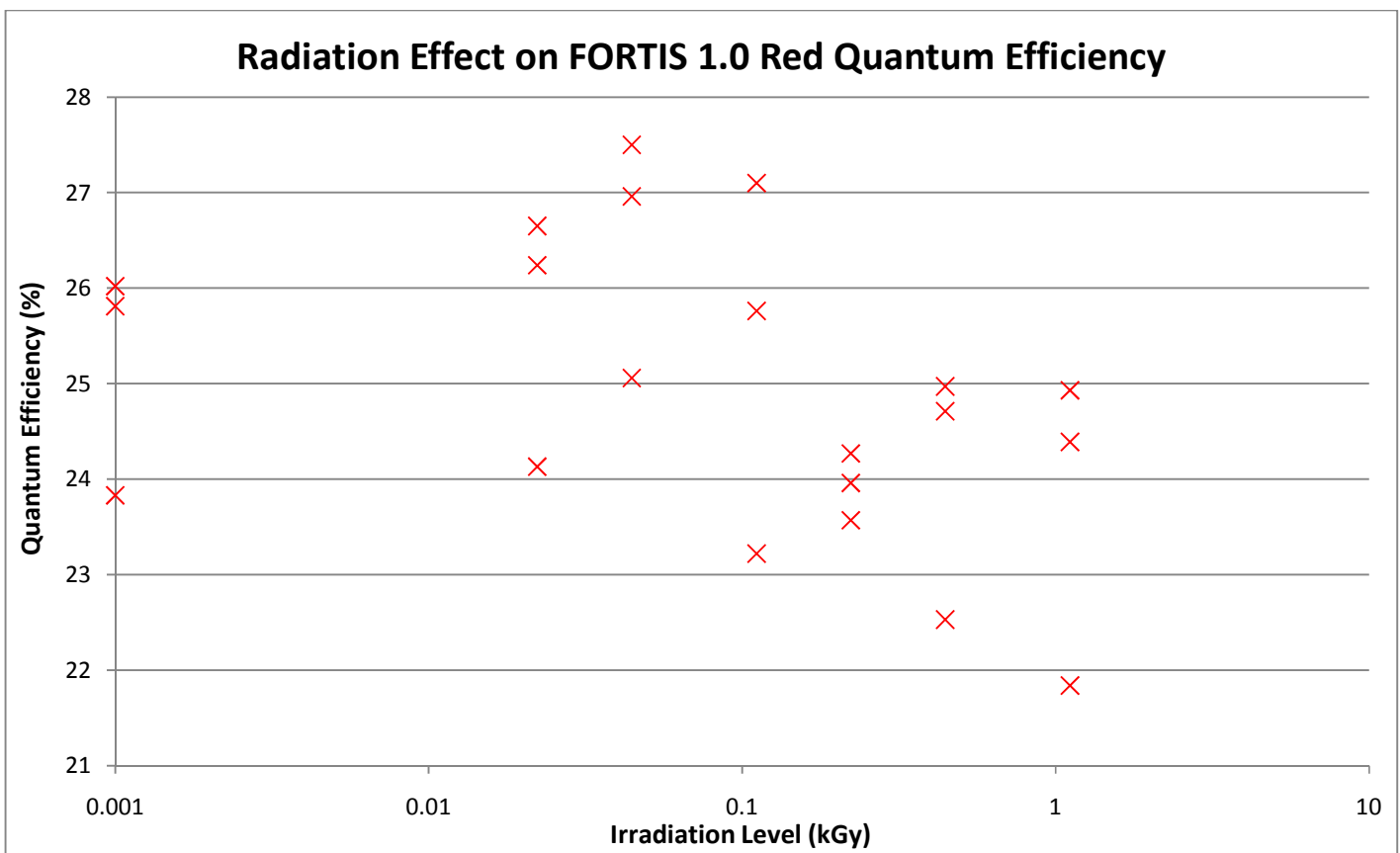


*Fig. 39 – Radiation hardness results for conversion gain*

The gain of the sensor does not change with radiation exposure. Within error, the results were essentially identical at all radiation levels, with the total range being approximately  $\pm 5\%$  of the average value. This suggests that the column readout circuitry has not been affected by radiation damage, which was expected because it was protected by the lead shield.

### (4.3c) Quantum Efficiency Results

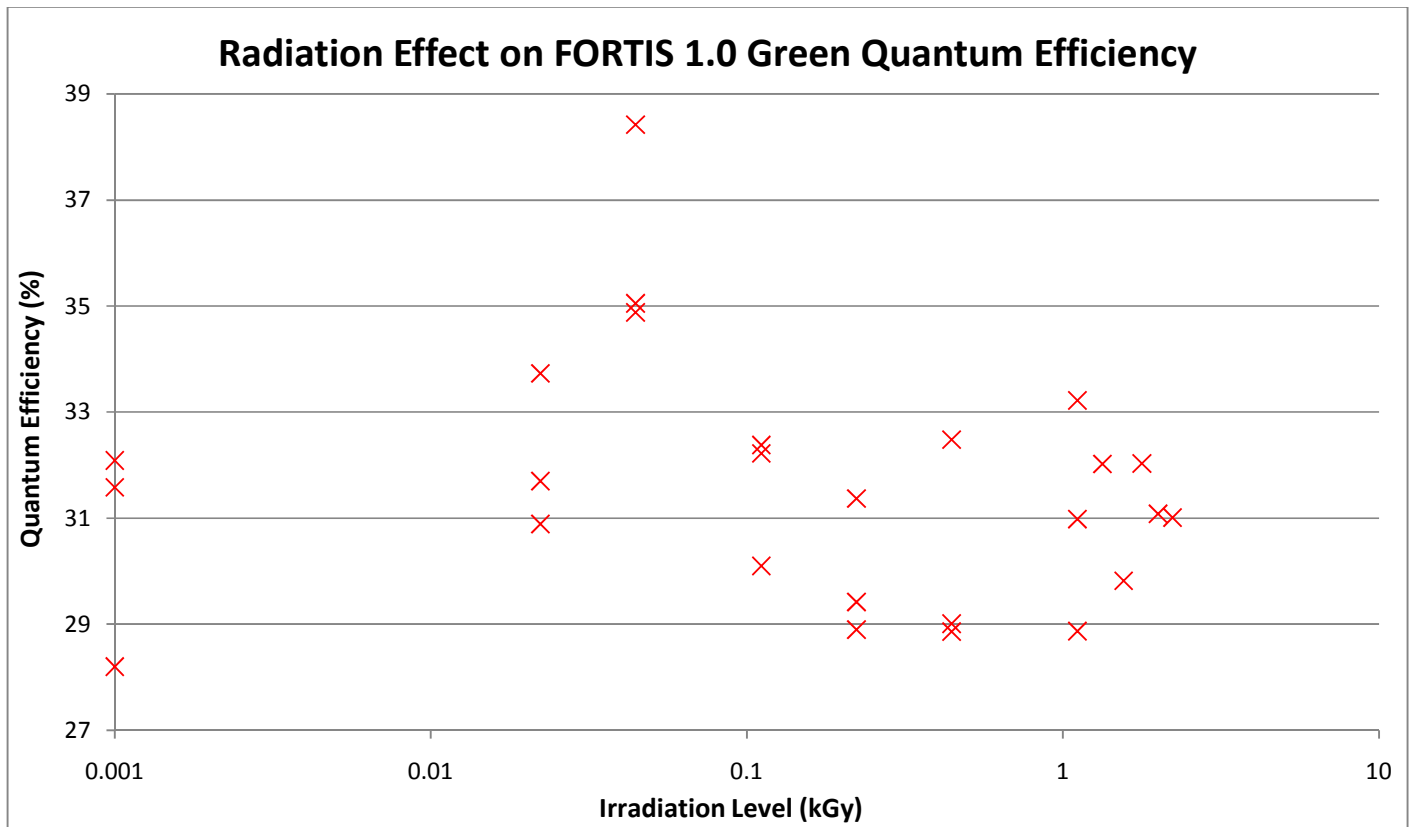
The third main parameter tested was quantum efficiency. These results are split into three graphs, one for each of the wavelengths tested: blue (470nm), green (546nm) and red (635nm) because the effect on each wavelength is different, unlike the noise and conversion gain results.



*Fig. 40 – Radiation hardness results for red quantum efficiency*

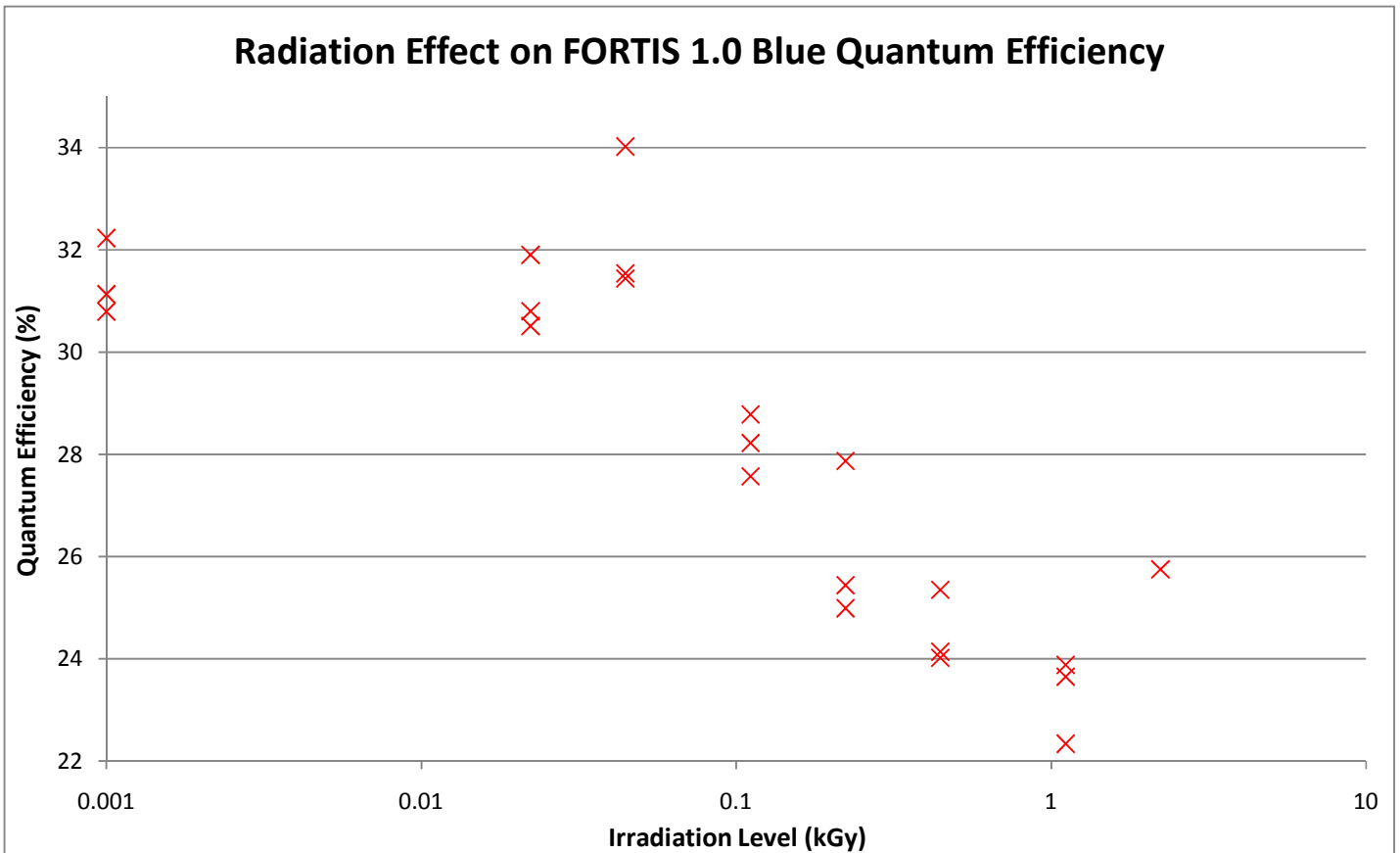
The trend for red light is difficult to determine. Although, on first inspection, it appears that there is a minor downward trend (the correlation not being as obvious as it was for noise), it seems that there is in fact no conclusive correlation because of the relatively large vertical gaps between each result. Although it is possible that a small decrease occurs, the shape of the graph could just be due to error in the results - quantum efficiency is one of the most difficult

parameters to measure accurately and using the per pixel analysis method is not completely ideal.



*Fig. 41 – Radiation hardness results for green quantum efficiency*

The trend for green light is even less evident than that of red light – a non-conclusive possible logarithmic decrease. There are a few more points on this graph beyond 1 kGy and they seem to agree with the fact that there is no real correlation.



**Fig. 42** – Radiation hardness results for blue quantum efficiency

Here we can see that the trend for blue light much more closely mirrors the noise results, with the parameter clearly getting worse with greater radiation exposure. Whereas the green quantum efficiency results mostly lie between 29% and 31%, the quantum efficiency under blue light ranges from 22% to 32%, even when excluding relative outliers such as the 34% point - a much larger difference.

The quantum efficiency doesn't appear to be affected until around 0.1 kGy but beyond here, there is a definite logarithmic decrease. The reason for the difference between each wavelength is likely due to the fact that blue light (in this case 470nm) does not penetrate the diode as deeply. It is possible that there are more shallow traps than deep ones in the oxide or it could be



a consequence of the pinned photodiode, which is more sensitive to blue light than higher wavelengths, being affected by radiation damage.

#### (4.3d) Dark Current Results

Fig. 43 below shows how dark current changes with radiation exposure.

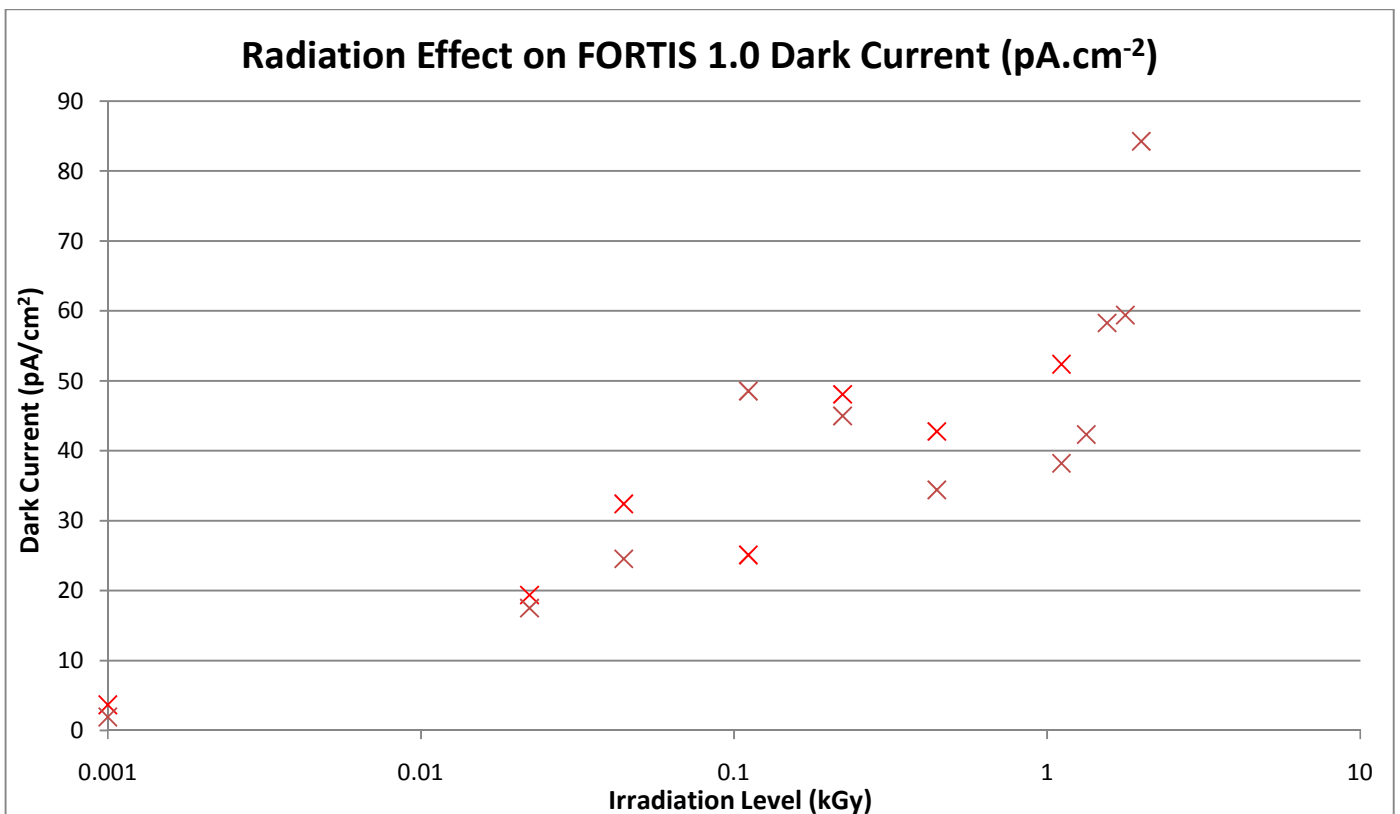
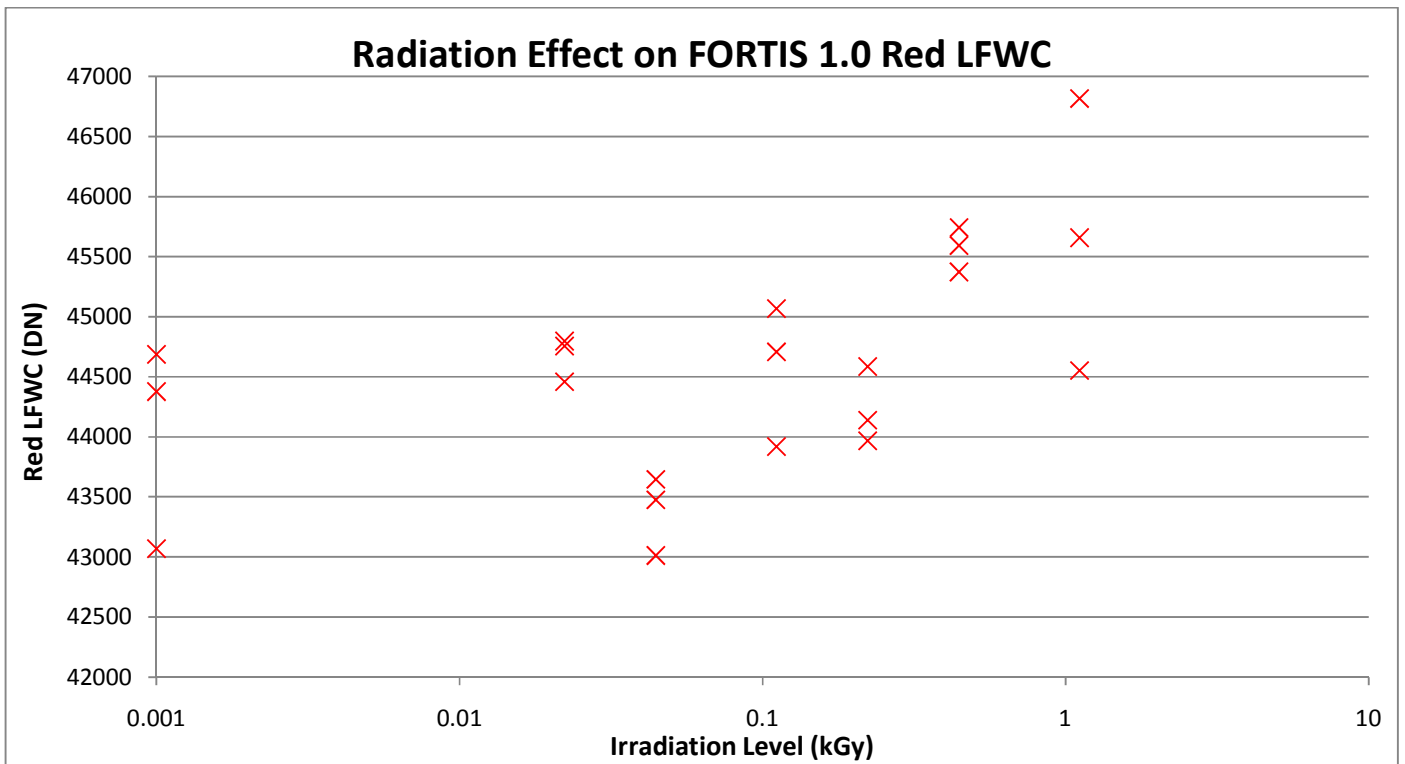


Fig. 43 – Radiation hardness results for dark current

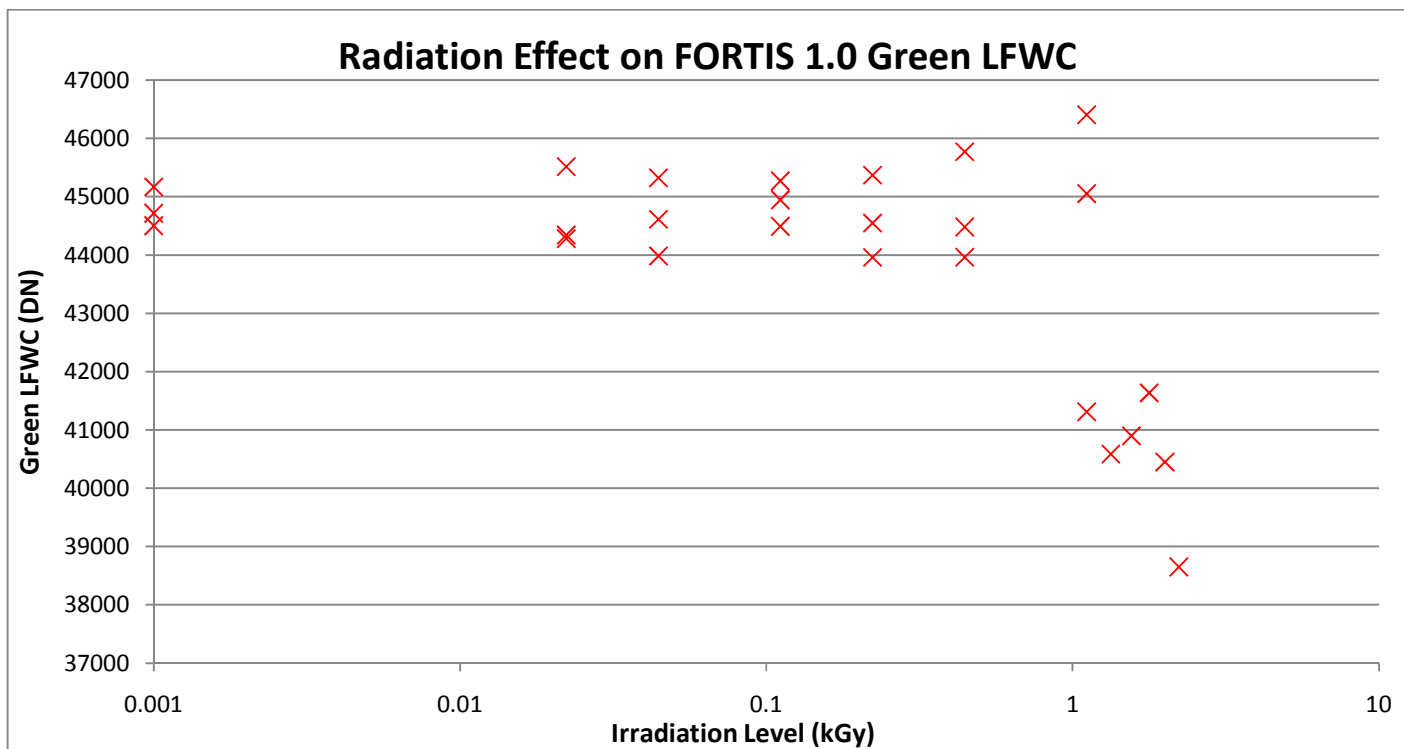
Once again, the dark current increases logarithmically, as expected<sup>[12]</sup>, probably due to the traps in the oxide. The increase is very significant (up to 4500% at 2.2 kGy) and is clearly a large contributing factor to the general increase in pixel noise.

#### (4.3e) Linear Full Well Capacity Results

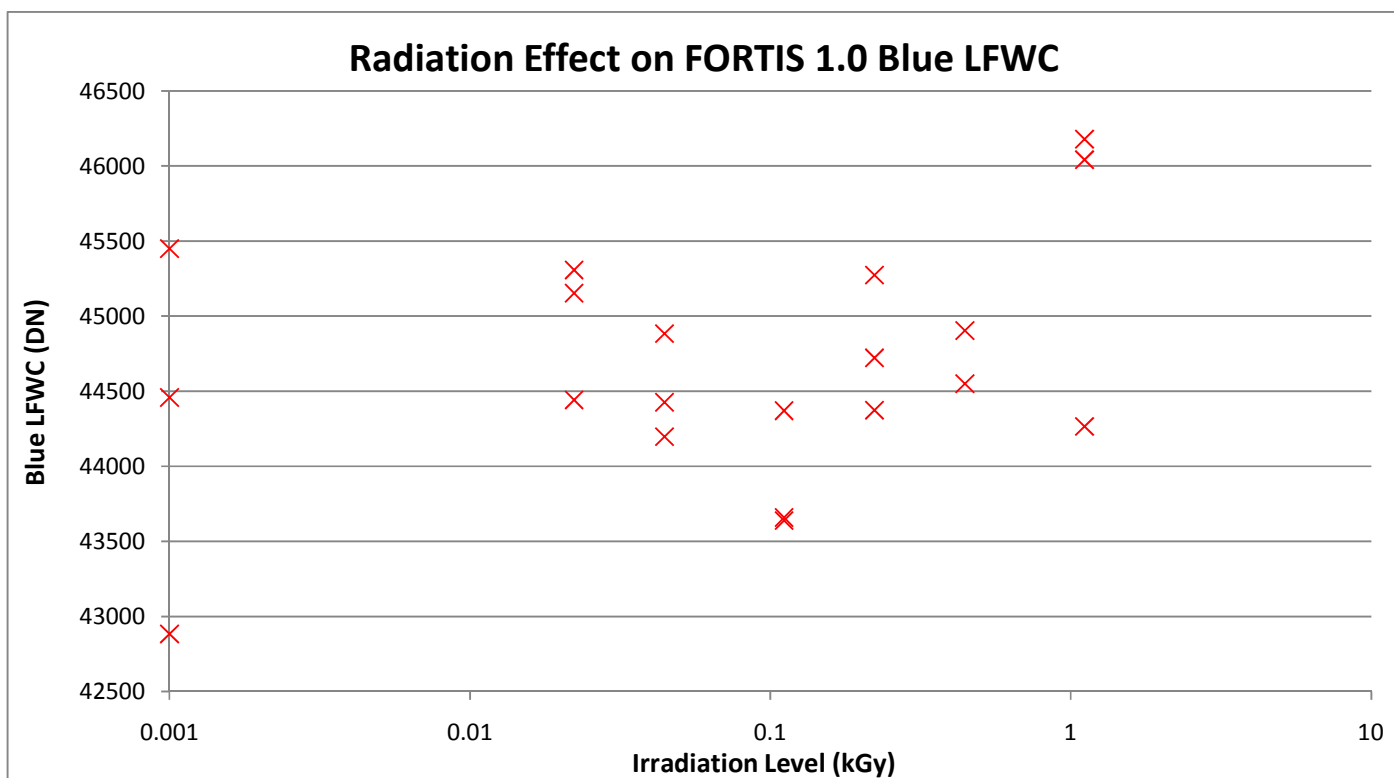
The following three graphs display the change in linear full well capacity (LFWC) under red, green and lastly blue light.



*Fig. 44 – Radiation hardness results for red maximum full well capacity*



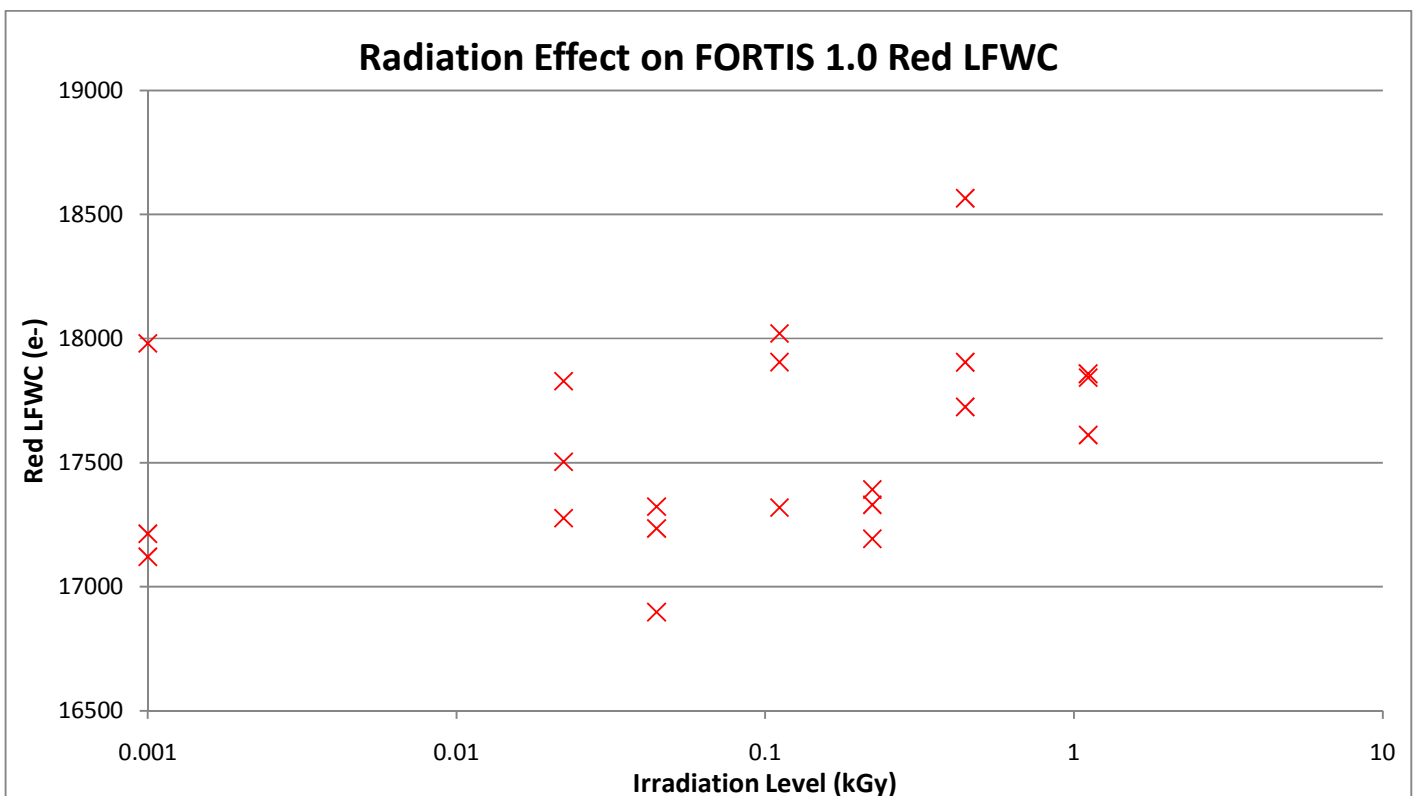
**Fig. 45** – Radiation hardness results for green maximum full well capacity



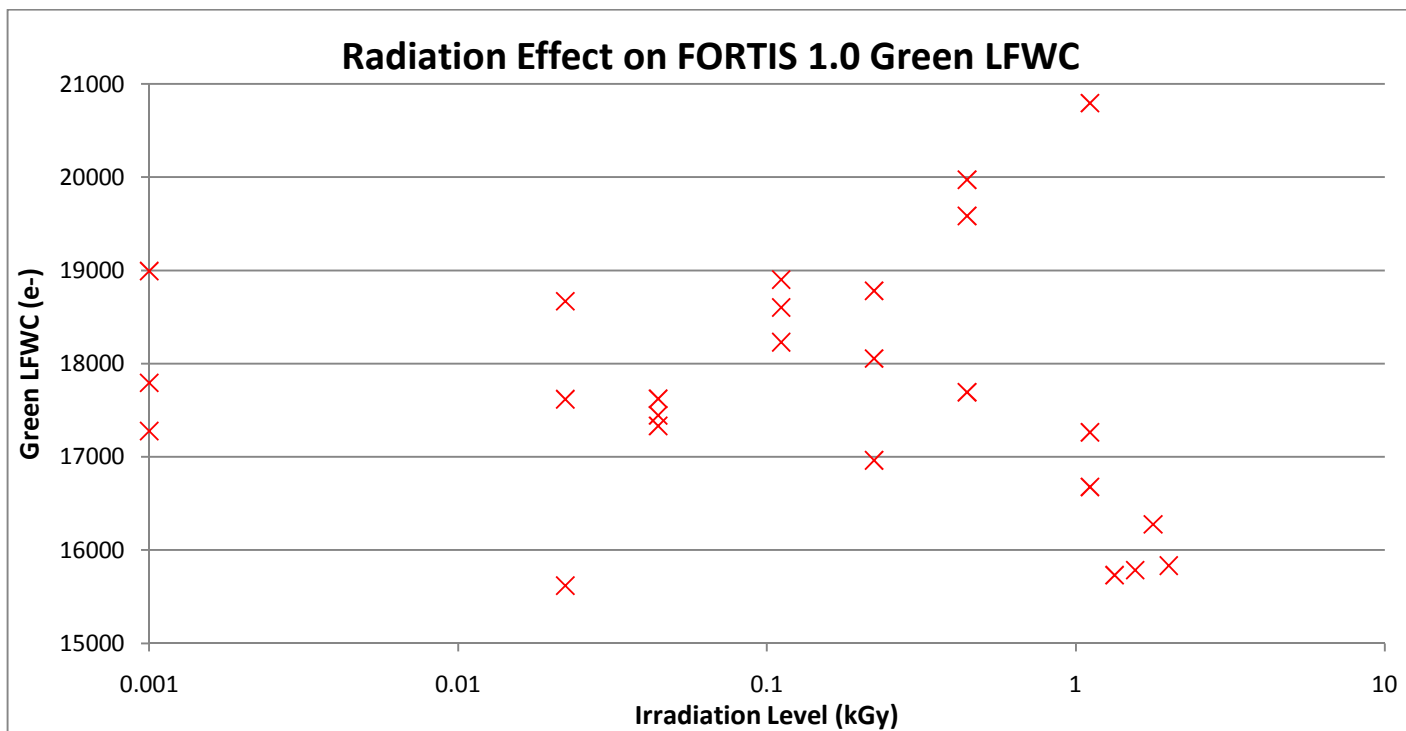
**Fig. 46** – Radiation hardness results for blue maximum full well capacity

On first inspection, the trend appears to be that the linear full well capacity slightly increases with radiation damage for red, decreases for green (especially after 1 kGy) and stays more or less constant for blue light. However, the increase is barely noticeable on a large scale, with *Fig. 45* (green light) being the only one that couldn't be accounted for by error ( $\pm 1\%$  due to the fluctuations seen in repeated measurements). There isn't really any reason that green light would be affected more than the other two – if anything, the blue light graph should decrease the most because of the increased number of shallow traps.

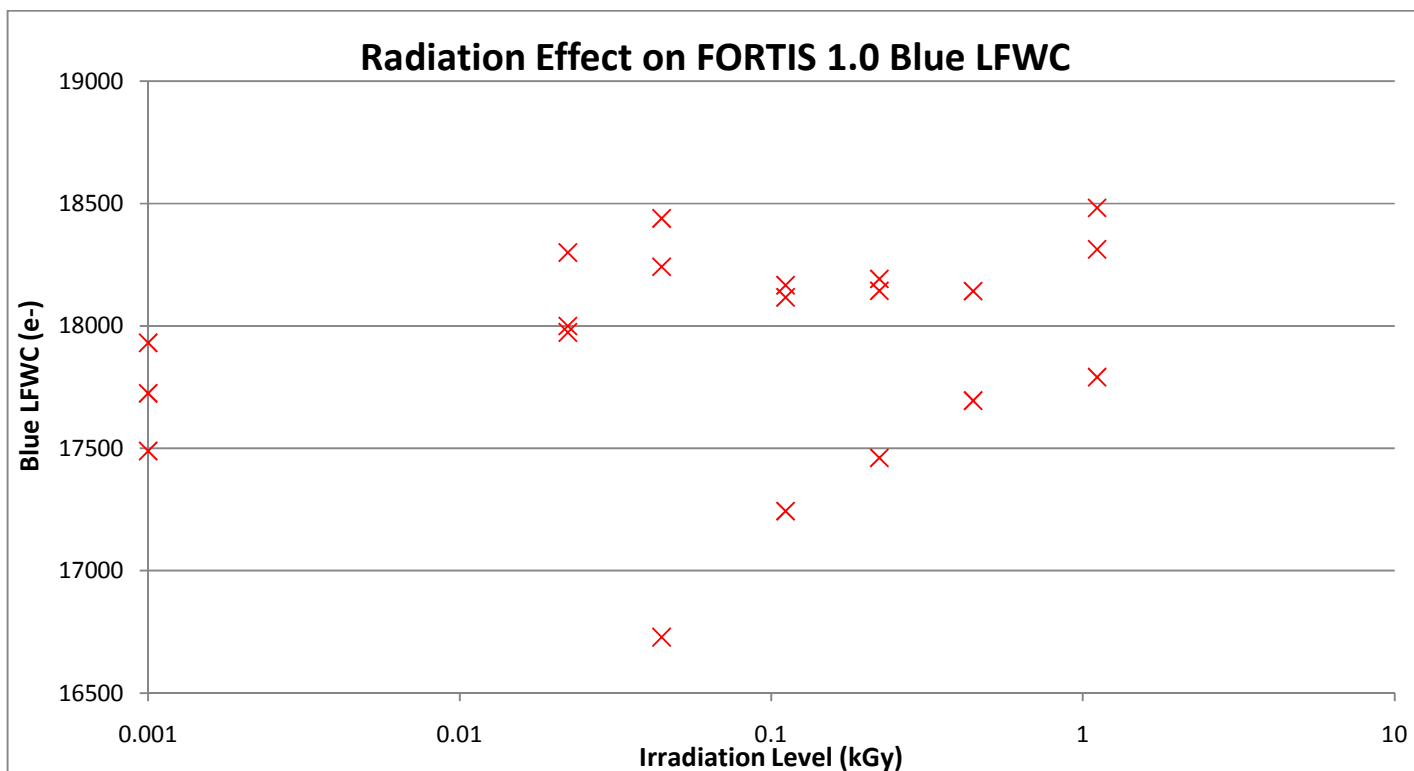
The situation becomes more interesting when we convert these graphs' y-axes from digital numbers to electrons using the previously obtained conversion gain.



**Fig. 47** – Radiation hardness results for red maximum full well capacity after conversion to electrons



**Fig. 48** – Radiation hardness results for green maximum full well capacity after conversion to electrons

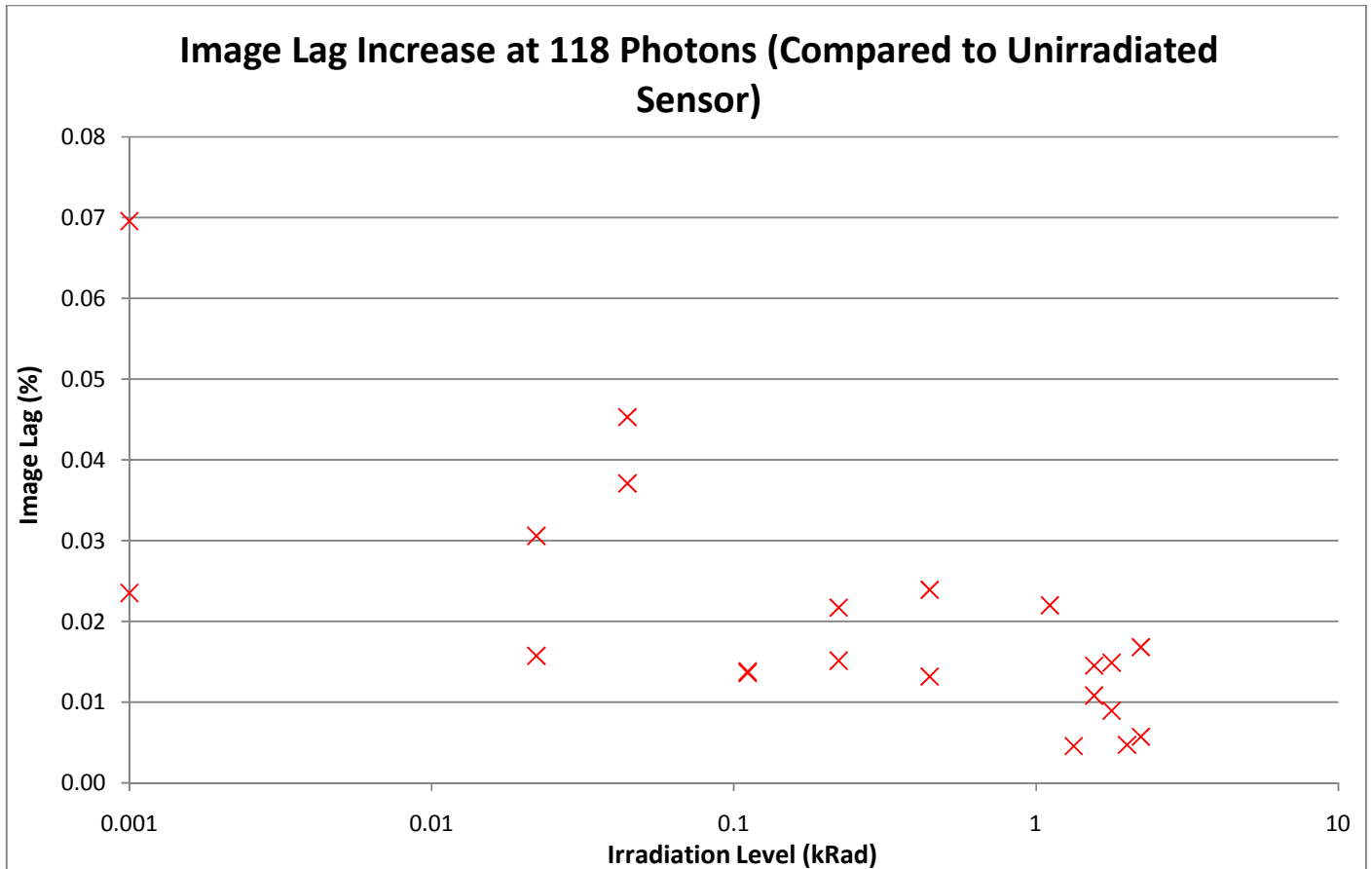


**Fig. 49** – Radiation hardness results for blue maximum full well capacity after conversion to electrons

Interpreting these graphs, there is no real trend at all for red, green or blue light. There are two explanations for this. The first is that the error in these results, which matches the full well capacity measurements from *Section 4.2*, accounts wholly for the “trend” seen in the digital number graphs (*Figs. 44-46*). The other is that if there is indeed a trend, it could simply be due to a minor shift in the output voltage, causing both the maximum and minimum output values from the sensor to decrease slightly whilst not affecting the actual linear full well capacity of the sensor in terms of detectable charge.

Although it is logical and likely that the full well capacity of FORTIS 1.0 decreased after 2.2 kGy of radiation exposure, the error in the results is too great to say that the graphs are conclusive. The annealing results however show a more discernable difference (see *Section 4.3g*).

#### (4.3f) Image Lag



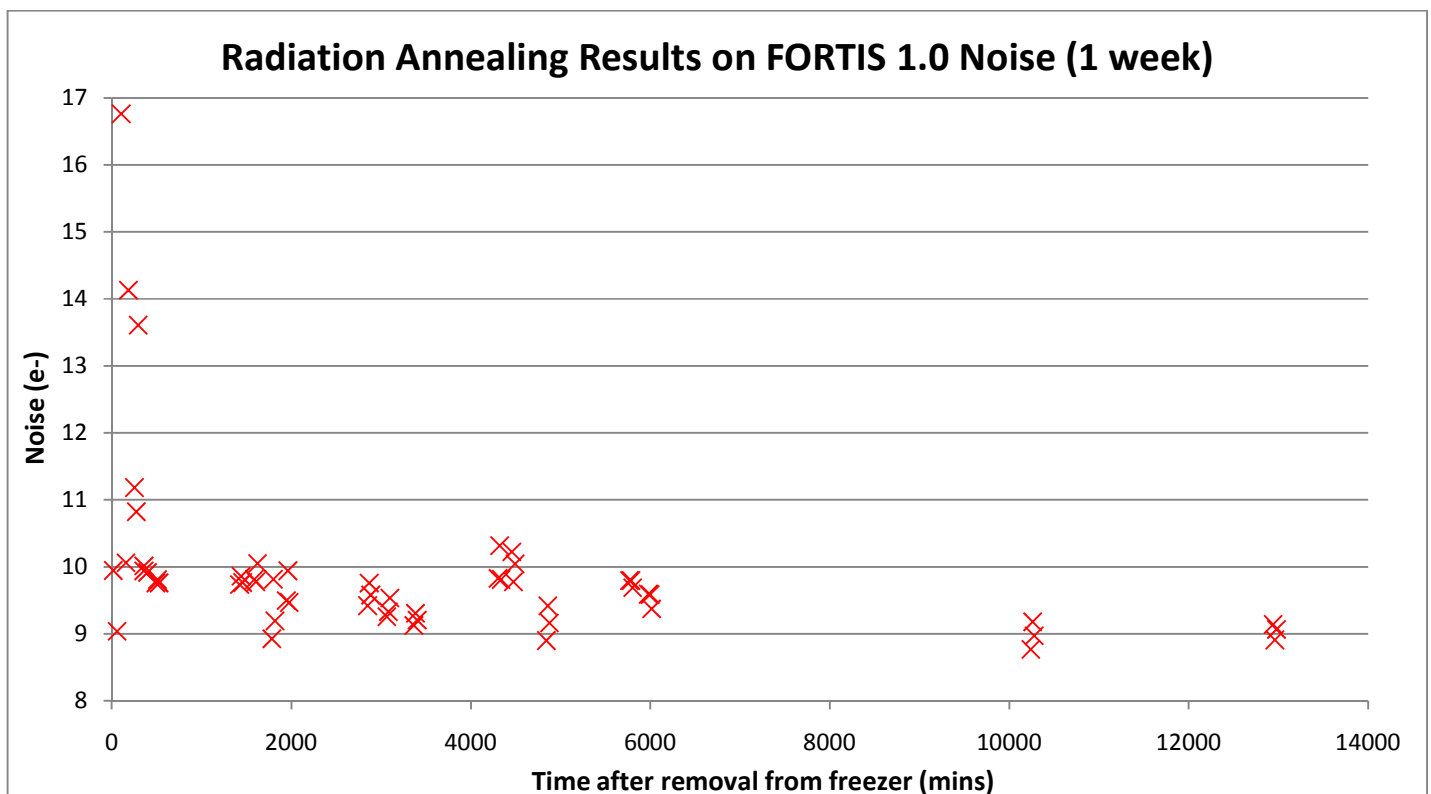
*Fig. 50 – Radiation hardness results for image lag*

The reason that the image lag at 118 photons was chosen is that it is sufficiently high enough to not be concealed by sensor noise. However, there is still an inherent error in the results because each measurement was taken from a different sweep. It is clear that the image lag increases after irradiation but the increase is extremely small and so difficult to quantify. There also doesn't appear to be any real trend so nothing more can be concluded from these image lag results.

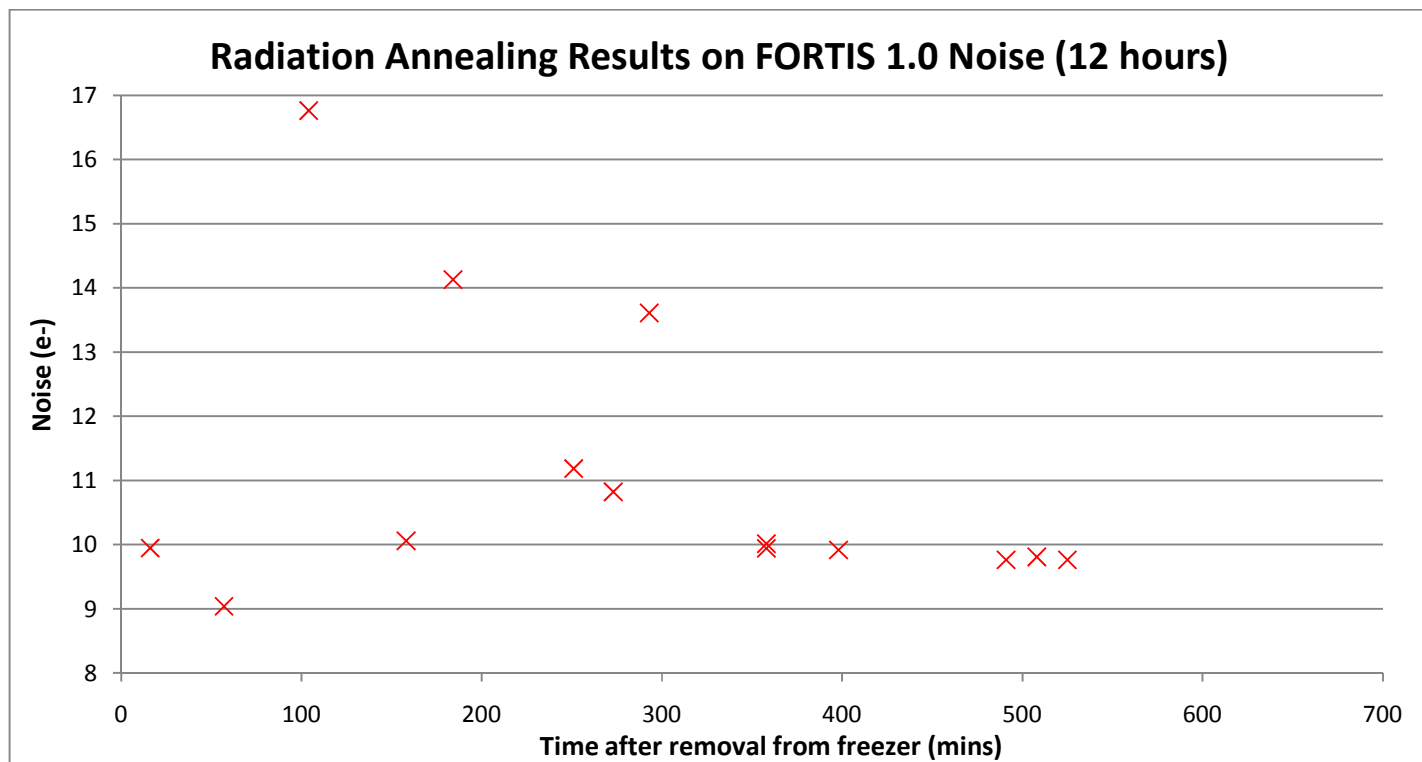
The method used for testing image lag involved using different same-length vectors that had the transfer gate open for different lengths of time. It was known that this method was far from ideal in terms of results and also the time taken to conduct such tests (several hours for a single image lag measurement) but it was the only one available to us at the time. New technology on Tester 2 allows for a superior technique to be used that is far more reliable as well as much faster. See *Section 5.1* for more details on this.

### (4.3g) Annealing Results

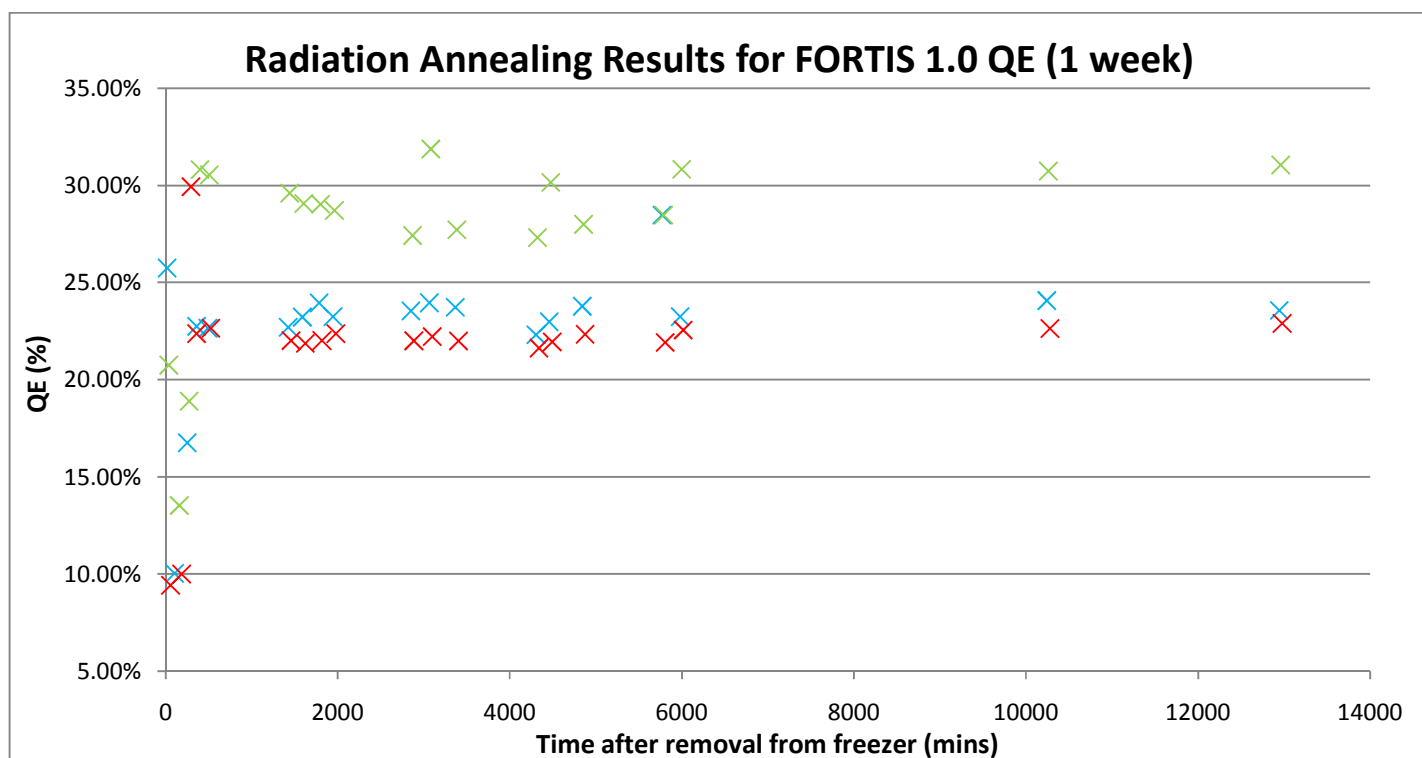
RAD2 was retested numerous times during the week following its 2.22 kGy exposure, without ever being placed in the freezer to slow down its annealing. The following graphs show the pattern of various results over the course of the first 12 hours as well as over the entire week.



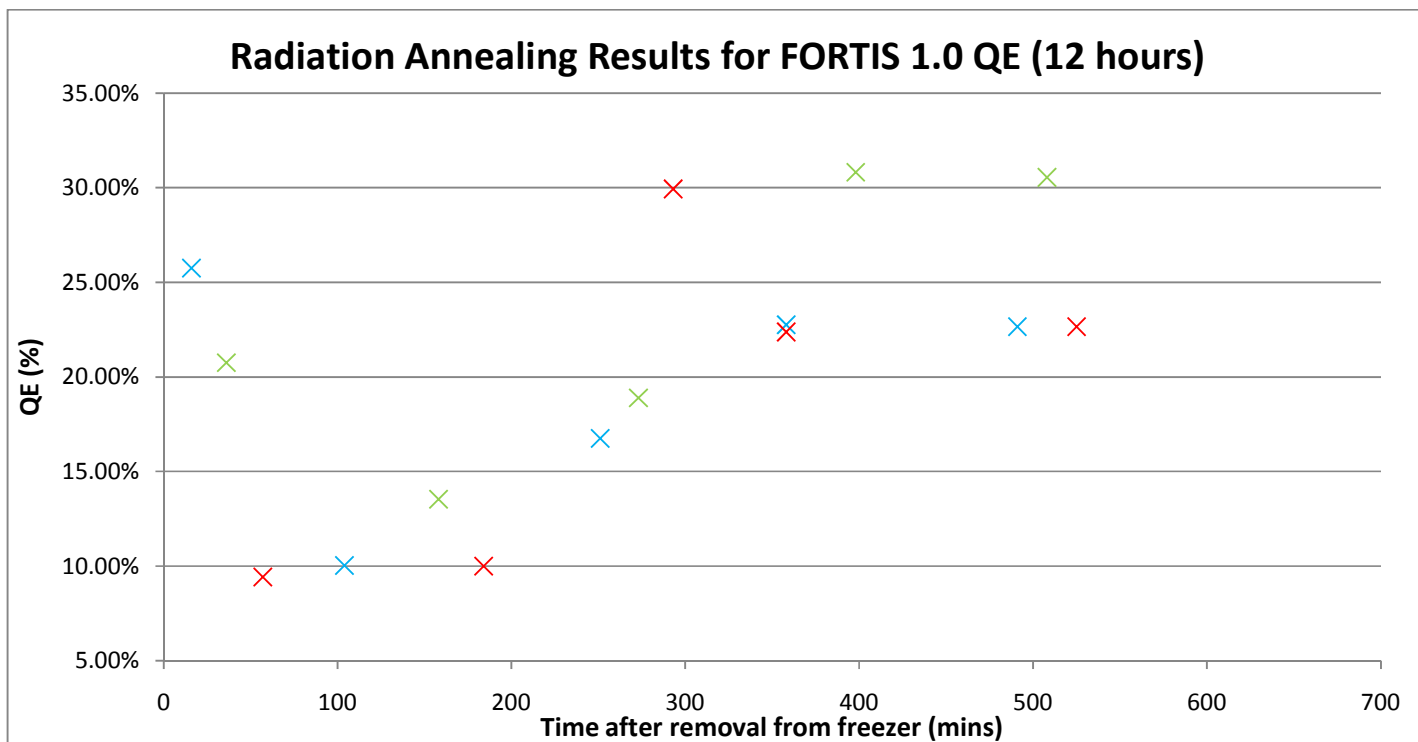




*Fig. 52 – Radiation hardness annealing results for noise over 12 hours*



*Fig. 53 – Radiation hardness annealing results for QE over 1 week*



*Fig. 54 – Radiation hardness annealing results for QE over 12 hours*

This set of annealing results is really interesting because all they all show similar characteristics. For the first hour after irradiation, the sensor’s performance is fairly normal. After around one hour, the sensor’s performance decreases similarly for noise and quantum efficiency. This was not an expected result but there is a plausible explanation for such behaviour – the sensors were not biased whilst being exposed to radiation (which would have been a more ideal test method). Thus, when the sensors are first biased and operating normally, the radiation effects (traps) could move around the sensor, exaggerating the detrimental effects.

Within twelve hours of irradiation, both the noise and quantum efficiency values level out and can be considered “full recovered” shortly after this.

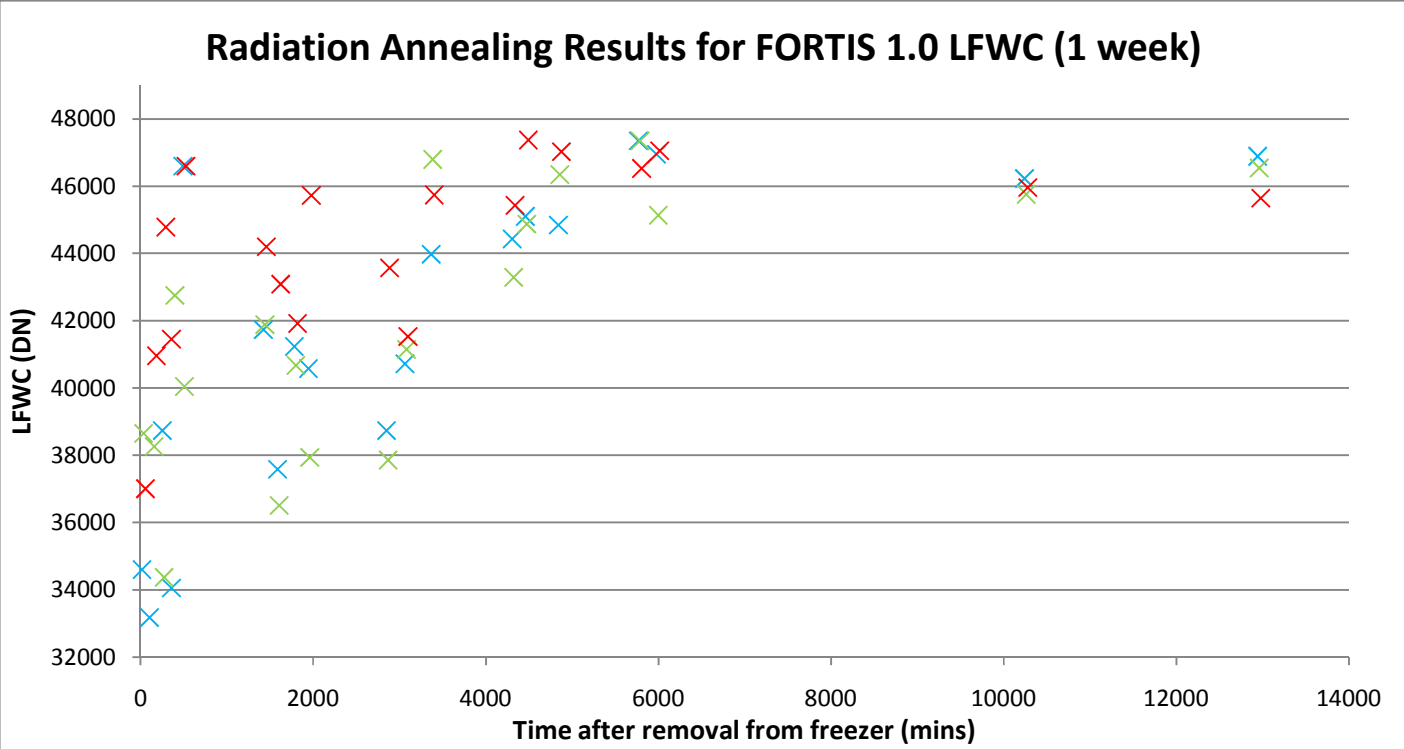


Fig. 55 – Radiation hardness annealing results for linear full well capacity over 1 week

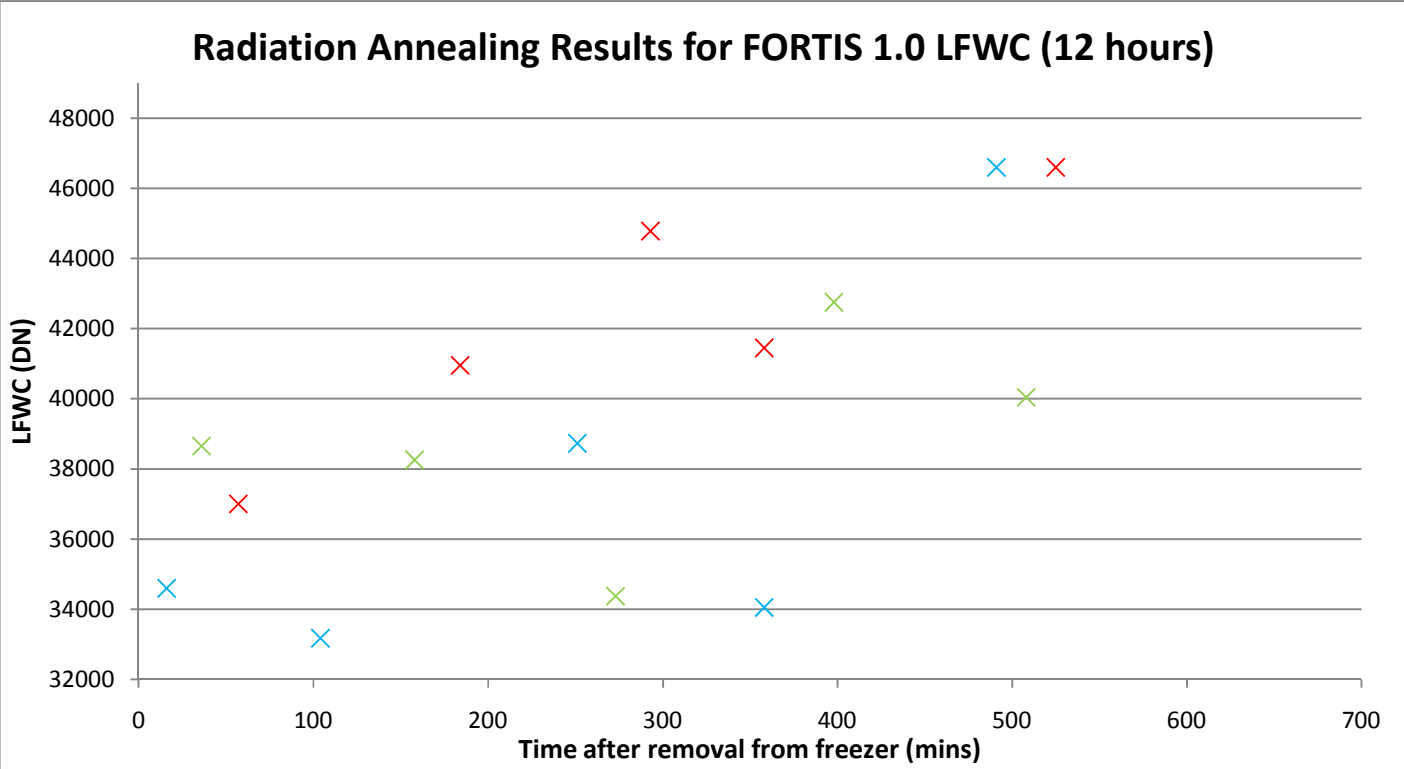
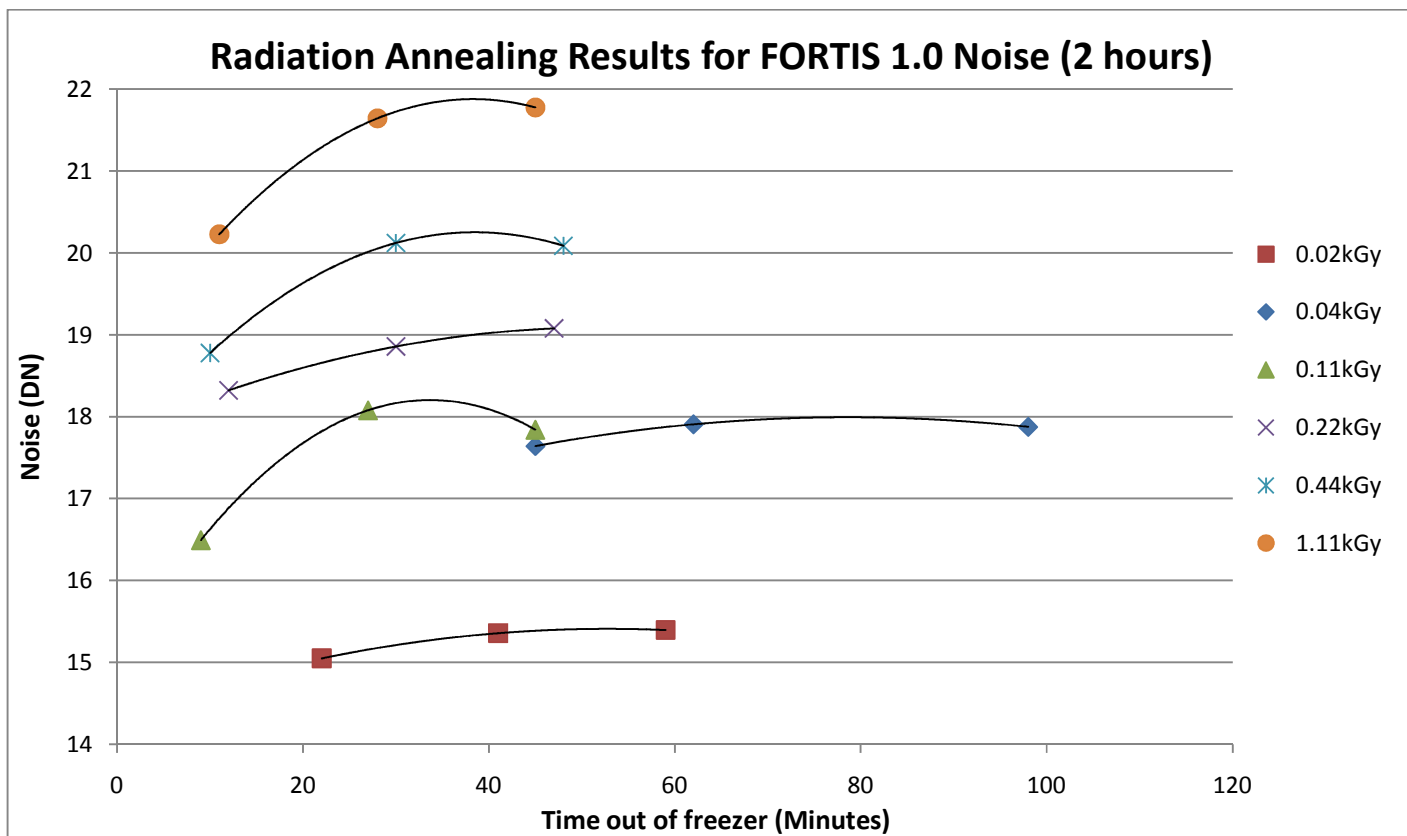


Fig. 56 – Radiation hardness annealing results for linear full well capacity over 12 hours

Here we see that the recovery of the sensor's linear full well capacity does not return to normal levels until much longer after the irradiation has completed. *Fig. 55* suggests that it takes ~5000 minutes (or 3.5 days) for the linear full well capacity to return to normal values. This is presumably because of lingering stray traps within the oxide, which limit the amount of detectable charge and may take a long time to diffuse.

These results tell us that the FORTIS 1.0 B2 pixel and surrounding output circuitry can withstand 2.2 kGy of radiation and fully recover given enough time. Indeed, the PTC of these sensors also returned to a normal shape at the end of the annealing period after being distorted by the radiation damage.

Interestingly, the normal radiation hardness test results from RAD2 show a similar pattern of noise increasing before improving, as shown in *Fig. 57* below. The reason such a graph can be generated is because each colour was tested in the same sequence every time a sensor had finished its irradiation cycle (blue, green then red). Because each colour test took a fixed length of time (20 minutes), the results of each colour could not be taken at exactly the same time after removal from the freezer.



*Fig. 57 – Radiation hardness annealing results for noise over 2 hours (from normal testing)*

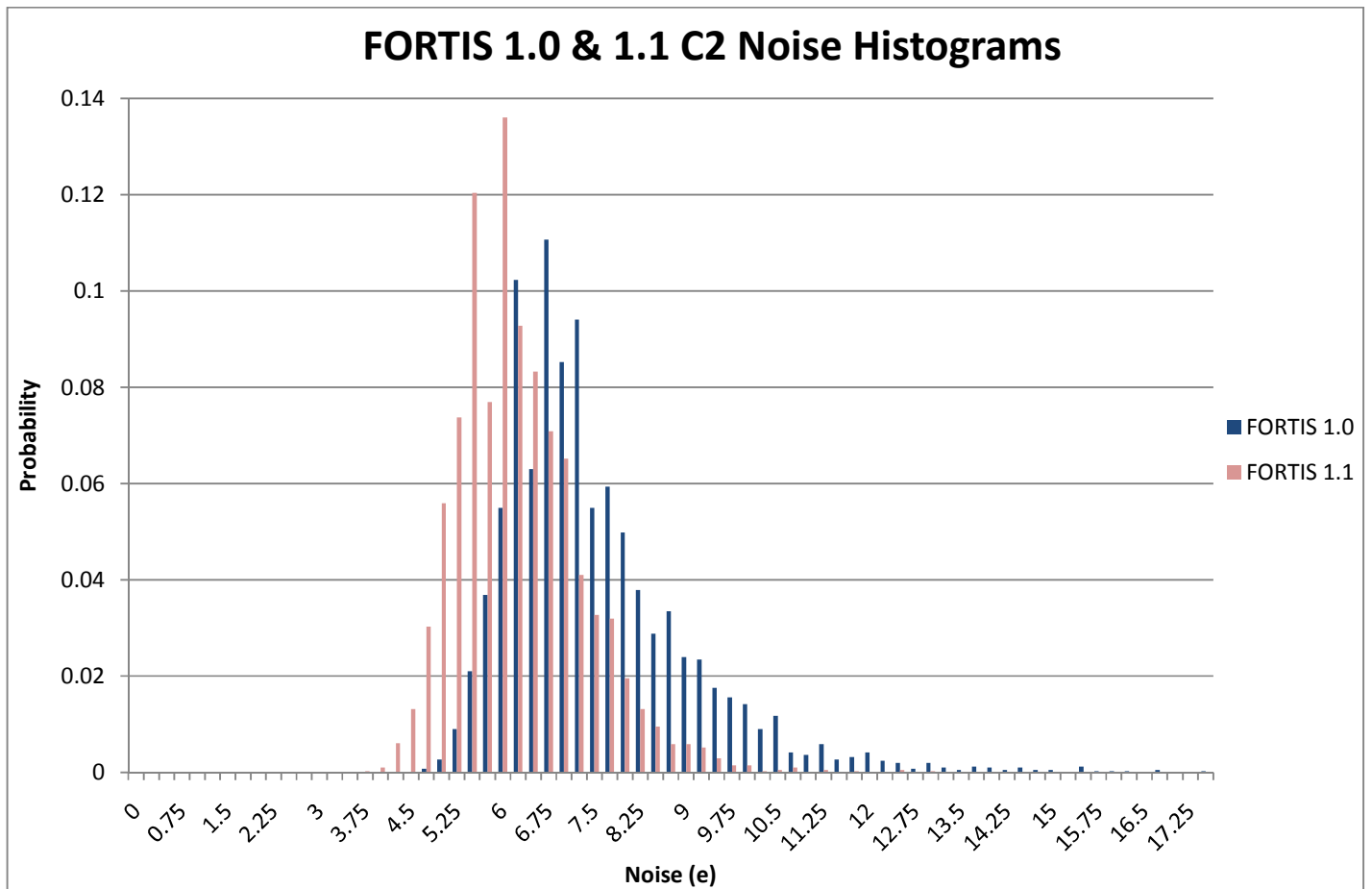
Noise should not be affected by colour so these results can be taken to somewhat mirror what was seen during the annealing tests. If the theory that the sensor being biased makes the radiation effects worse before the sensor recovers is correct, the time between removal from the freezer and the first test should not matter too much (unless it was so long that the sensor could recover fully before use). Unfortunately, because annealing effects were not under consideration during the general radiation hardness testing, the time between removal from the freezer and the first test was consistent between each test, except for 0.04 kGy. Unfortunately, the 0.04 kGy noise results are too close together (and so the trend could easily be due to noise) to help prove this theory.

#### **(4.4) FORTIS 1.0 & 1.1 COMPARISON**

Unfortunately, only one of the three previously available pixel arrays on FORTIS 1.0 was also available to be tested on FORTIS 1.1. This pixel was C2. As can be seen from the FORTIS 1.0 results (see *Section 4.2*), C2 performed similarly to B2 although it had nearly double the noise and a slightly reduced conversion gain because of the differently sized source follower.

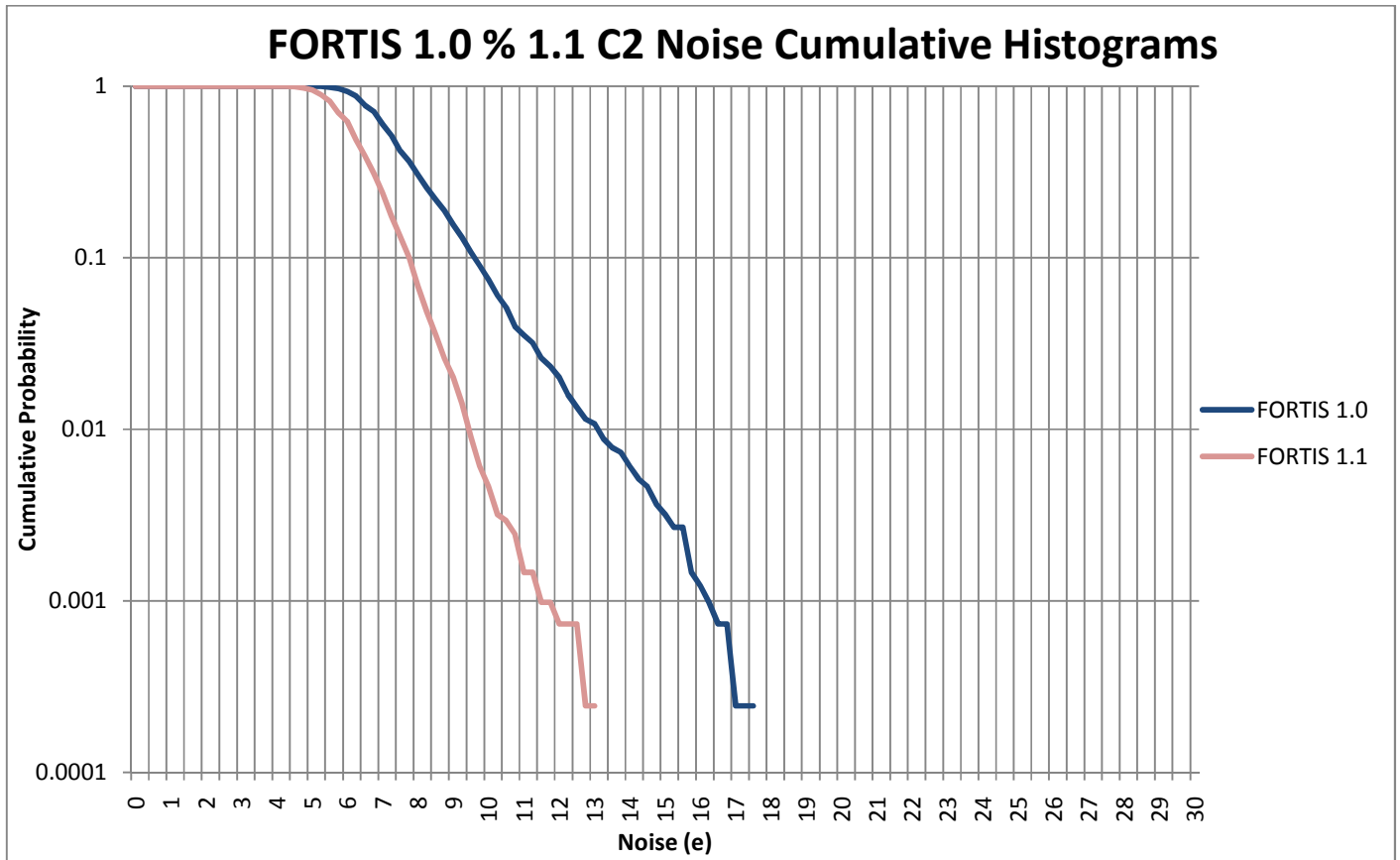
In terms of sensor design, the C2 pixel arrays on a FORTIS 1.0 and FORTIS 1.1 sensor are identical. However, the foundry offered to use a special low-noise implant for the main (“control”) processing variation of FORTIS 1.1. It was decided to therefore test the actual effect this would have on the C2 pixel array’s noise (after optimisation). Because the foundry’s low-noise implant is proprietary and was not explained, this test will not show anything other than whether the implant is worth using for future sensor designs.

The initial average noise results showed that the low-noise implant did in fact reduce the noise, from an average of  $(8.7 \pm 0.5)$  electrons to  $(6.9 \pm 0.5)$  electrons. *Fig. 58* below shows a histogram comparison of pixel noises within a 64x64 sized C2 array for FORTIS 1.0 and 1.1.



*Fig. 58 – Histograms for FORTIS 1.0 & 1.1’s C2 noise*

The FORTIS 1.1 histogram is shifted to the left, indicating a higher probability of pixels with noise below 6 electrons. The histogram also appears thinner, with a shorter “tail”, which represents a lower probability of unusually high noise pixels (above 10 electrons). This comparison is made clearer when looking at the cumulative probability histogram in *Fig. 59*.



**Fig. 59** – Cumulative histograms for FORTIS 1.0 & 1.1's C2 noise <sup>[16]</sup>

The red line not only decreases earlier but it also is steeper, mirroring the narrower and shifted histogram seen in Fig. 58. As well as the reduction in the average noise, the maximum noise for a single pixel is also reduced significantly from  $(17.5 \pm 0.5)$  electrons to  $(13.0 \pm 0.5)$  electrons, which represents a reduction in random telegraph signal noise <sup>[16]</sup>. From these graphs we can conclude that the low-noise implant does indeed reduce real-world noise by a good margin and is superior to the untreated FORTIS 1.0.



## (5) CONCLUSIONS

FORTIS 1.0 had three of its pixel arrays optimised and characterised. Pixels B2 and C2 proved to have very good performance, especially in terms of conversion gain ( $(2.47 \pm 0.02)$  DN/e and  $(1.69 \pm 0.02)$  DN/e respectively) and quantum efficiency ( $(31.0 \pm 0.2)$  % and  $(31.9 \pm 0.2)$  % respectively). The differences between these two pixel arrays was the shape of their active area – B2's being L-shaped and C2's being straight – as well as C2's larger source follower. These may have been the cause of the relatively large discrepancy in their noise values -  $(6.2 \pm 0.5)$  electrons for B2 and  $(10.8 \pm 0.5)$  electrons for C2, on average. A larger source follower could increase fixed pattern noise and it appears that this effect outweighed the fact that random telegraph signal noise should have been reduced.

The higher floating diffusion node capacitance present in the A2 pixel resulted in a pixel that performed worse in all three of the priority parameters, suffering a ~63% decrease in quantum efficiency and conversion gain when compared to the B2 pixel, as well as a 232% increase in noise. This showed that the foundry's original 6  $\mu\text{m}$  pixel design stretched to 15  $\mu\text{m}$  did not perform as well as their newer native 15  $\mu\text{m}$  pixel design (as used in all pixel arrays except for A1 and A2).

FORTIS 1.0's B2 pixel was tested for radiation hardness. Its noise and dark current decreased logarithmically with radiation exposure, whereas its conversion gain and linear full well capacity appeared unaffected (when expressed in electrons). The quantum efficiency was the strangest result – in blue light, it decreased logarithmically once the radiation level reached ~0.1 kGy but in red and green light, there was no discernable trend. It was concluded that this was likely due

the fact that more shallow traps were created by the bombardment of radiation, which would have a far greater effect on incoming blue light than red or green. The pinned photodiode may also have suffered damage, which again would affect blue light more so than red and green.

The radiation annealing experiment was important because it showed two important things. Firstly, that the sensor was able to fully recover when given enough time after 2.22 kGy of radiation exposure. Secondly, the biasing of the sensor after testing greatly affected the obtained results. It was decided that it is important for the sensor to be biased during future radiation hardness tests in order to ensure that suddenly biasing after the exposure (i.e. during testing) does not skew results. This would also be a more realistic simulation of radiation damage during common applications involving electromagnetic radiation and other ionising particles.

Image lag was tested at various levels of irradiation and compared to a presumed 0 lag test with a non-irradiated sensor. The results were difficult to analyse and the method was deemed insufficient. Future image lag tests will be done with Tester 2's new "flash" ability, which should provide better results (see *Section 5.1*).

It is important to note that temperature theoretically affects some sensor properties, in particular dark current. This was not made part of the testing because preliminary tests with a temperature sensor placed as close to the sensor as possible showed that over the course of normal intensity and integration sweep tests, the temperature changed by less than 0.1°C, which should not be enough to affect results in a measurable way.

To summarise, the FORTIS 1.0 B2 design produced the lowest noise of any sensor created by the CMOS Sensor Design Group at RAL, the best result being  $(5.7 \pm 0.5)$  electrons. When the noise results for the radiation hardness sensors prior to irradiation are combined with those of the initial three test sensors (a total of 12 measurements), the average decreases to  $(6.0 \pm 0.5)$  electrons. It looks to be promising for applications where high sensitivity to low charges is important (due to both its low noise and high conversion gain), such as many areas of particle physics. Its tolerance to decently high levels of radiation (at least 2.22 kGy) also makes it good for such applications because it has been proven that it can recover from such levels. In real applications, radiation doses are much lower (i.e. more spread out so a radiation level will be reached within a year rather than a day, for example), which generally allows the sensor to recover with greater ease than when given a large dose in a short period of time and not allowed to anneal. Radiation hardness testing with FORTIS 1.1 will continue to higher levels as a continuation of this study – in particular, we were unable to determine the level at which the sensor becomes irreversibly damaged, which would be of great interest.

The effect of FORTIS 1.1's low-noise implant (used for the control processing variation) was also tested. Because the only pixel type available on both revisions of the sensor was C2, this pixel was chosen for the comparison. The average noise decreased by a very decent 20% and the maximum noise for a single pixel was reduced by a significant 26%. The cumulative histogram confirmed that the number of pixels with unusually high noise was indeed reduced by a noticeable amount. Conversion gain was also increased by this process, although that test was

not included in this project <sup>[16]</sup>, leading the conclusion that this specialised process would indeed be a good inclusion for future similar sensors.

### **(5.1) OTHER TASKS AND FUTURE TESTING**

The main task during my placement aside from testing FORTIS 1.0 and 1.1 was the development and incorporation of a revamped version of the *per pixel analysis* software that was used for analysing sensor sweep data. The details of the advantages of this new version are discussed in *Section 3.3a*. The program was generally completed in July 2009 and was presented to the other members of the CMOS Sensor Design group. During this presentation, several enhancements were suggested and discussed. Among these was the addition of a better way of calculating dark current (including the addition of dark transfer curve, DSNU and PRNU graphs), a full-width half-maximum calculation for the dark-corrected signal histogram, an option to change the best-fit method used for all of the graphs, and an output of histograms for noise, quantum efficiency, gain, dark current, maximum full well capacity, linear full well capacity and the  $R^2$  value from the pixel's PTC best-fit line.

One major problem with the *per pixel analysis* program was the size of array that it could work with. The maximum image size that would work reliably was approximately 512x512 pixels and this was only possible on Tester 2, which had more RAM. There were two ways to solve this problem, the first of which was to upgrade the LabVIEW version on Tester 2 to a new 64-bit version (removing the 2GB per-application RAM limit of 32-bit applications) and perhaps also install more RAM. The problems with this solution are cost and the fact that it would likely break compatibility with aSpect's idVIEW software but it may be done in the future. The second

solution would be to rewrite the code that handles the data itself so that data is only read and kept in RAM when completely necessary. However, this solution was also unviable because it would greatly reduce the speed of the application and also produce far more complex code, particularly in a visual language such as LabVIEW.

The usability upgrade to the testers during the aSpect visit in May 2009 was very successful in reducing the amount of time spent setting up and performing sensor tests. The new system was not documented, so work on creating a user guide (in a similar style to the one created for the new *per pixel analysis* program) was started and nearly completed before my research year ended. Furthermore, an important element of the system upgrade was not completed during my time at RAL: the implementation of automatic loading of optimised voltages for a particular test setup or operation mode. Hopefully in the near future, optimised voltages will be able to be stored in, and loaded from, the same configuration files that currently contain the frame size and clock speed so that they will not have to be noted down and applied manually each time the vector is loaded.

FORTIS 1.1 was made on 7 processing variations, investigating the effects of technologies such as buried channels and deep P-well, high resistivity substrates. FORTIS 1.1 testing started in mid-2009 but several changes were made to the optimisation process and the final characterisation of all of the nine available pixels started later in the year (and continues now). It is scheduled to undergo radiation hardness testing in March 2010. These tests will be more exhaustive than those done for FORTIS 1.0; a list of changes for FORTIS 1.1's testing plan for is shown below:

- Each sensor will only be irradiated once. After testing, it will be discarded and the sensor board will be rebonded to another sensor. This requires more sensors to be used but will provide a more accurate set of results due to the lack of additional annealing and stepped exposure.
- Sensors will be biased during irradiation. Various biasing conditions will be tested (e.g. standard, grounded, full clocking). A cable will be added to the setup in between the sensor board and stack so that the testing apparatus can be separated in order to not be affected by the radiation. Extra shielding may also be required.
- Image lag will be tested using the new “flash” method on Tester 2, which enables and disables the LED light source with very precise timing and records various readings from the sensor at regular intervals during and after the flash. This method is incredibly fast compared to the one used for FORTIS 1.0 (both in setup and actual measurement) and should also be more reliable and easier to extract results from.
- Testing will span more than one processing variation as well as pixel arrays with different source follower and diode sizes. The high resistivity processing variation should improve radiation hardness but mainly protects against bulk damage so the effects may not be seen.
- In addition to testing with red, blue and green light, parameter changes under infra-red light (950nm) will also be tested.
- Current consumption of the digital power supplies will be tested at various levels of radiation damage.

- The dose rate will be varied. For example, an exposure of 1 kGy might be tested at three different dose rates to see if the sensor's performance parameters are affected differently.

Lastly, FORTIS 1.0 and 1.1 have recently returned from a beam test at CERN. Both control and high resistivity processing variations were involved in the test and both sets of results are in the process of being analysed to hopefully reveal the benefits of high resistivity substrates.

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## APPENDIX A: Pixel Structure Summary

|                      | A2                    | B2            | C2            |
|----------------------|-----------------------|---------------|---------------|
| Pixel Design         | 6µm stretched to 15µm | Modified 15µm | Modified 15µm |
| Array Size (pixels)  | 128 x 128             | 128 x 128     | 128 x 128     |
| Active Area Shape    | L-Shaped              | L-Shaped      | Straight      |
| Source Follower Size | Standard              | Standard      | Long          |

Table 3 – Summarised differences between the three pixel types tested in this project

## APPENDIX B: FORTIS 1.0 Optimised Timings and Voltages

| A2                              |  |                        |                        |                        |
|---------------------------------|--|------------------------|------------------------|------------------------|
| TIMINGS (μs)                    |  |                        |                        |                        |
| Integration time used for sweep |  | 67008000               |                        |                        |
| SAMPLE_S                        |  | 3                      |                        |                        |
| SAMPLE_R                        |  | 3                      |                        |                        |
| RESET                           |  | 16                     |                        |                        |
| TX1                             |  | 14                     |                        |                        |
| VOLTAGES (V)                    |  | Processing Variation 1 | Processing Variation 2 | Processing Variation 3 |
| VLOADBIAS                       |  | 2.650                  | 2.600                  | 2.550                  |
| VBIAS1                          |  | 2.600                  | 2.550                  | 2.125                  |
| VCOLBIAS                        |  | 2.120                  | 2.100                  | 1.725                  |
| VFLUSH_LOW                      |  | 1.350                  | 1.350                  | 1.300                  |
| VRESET1_LOW                     |  | 1.250                  | 1.250                  | 1.200                  |

Table 4 – Final A2 optimisations for initial test chips

| B2                              |  |                        |                        |                        |
|---------------------------------|--|------------------------|------------------------|------------------------|
| TIMINGS (μs)                    |  |                        |                        |                        |
| Integration time used for sweep |  | 16108000               |                        |                        |
| SAMPLE_S                        |  | 8                      |                        |                        |
| SAMPLE_R                        |  | 8                      |                        |                        |
| RESET                           |  | 8                      |                        |                        |
| TX1                             |  | 6                      |                        |                        |
| VOLTAGES (V)                    |  | Processing Variation 1 | Processing Variation 2 | Processing Variation 3 |
| VLOADBIAS                       |  | 2.200                  | 2.200                  | 2.200                  |
| VBIAS1                          |  | 2.450                  | 2.450                  | 2.450                  |
| VCOLBIAS                        |  | 2.350                  | 2.350                  | 2.350                  |
| VFLUSH_LOW                      |  | 1.400                  | 1.400                  | 1.400                  |
| VRESET1_LOW                     |  | 1.310                  | 1.320                  | 1.320                  |

Table 5 – Final B2 optimisations for initial test chips

| C2                              |                        |                        |                        |
|---------------------------------|------------------------|------------------------|------------------------|
| TIMINGS (μs)                    |                        |                        |                        |
| Integration time used for sweep | 16108000               |                        |                        |
| SAMPLE_S                        | 8                      |                        |                        |
| SAMPLE_R                        | 8                      |                        |                        |
| RESET                           | 8                      |                        |                        |
| TX1                             | 6                      |                        |                        |
| VOLTAGES (V)                    | Processing Variation 1 | Processing Variation 2 | Processing Variation 3 |
| VLOADBIAS                       | 2.260                  | 2.260                  | 2.260                  |
| VBIAS1                          | 2.100                  | 2.100                  | 2.100                  |
| VCOLBIAS                        | 2.370                  | 2.370                  | 2.370                  |
| VFLUSH_LOW                      | 1.400                  | 1.400                  | 1.400                  |
| VRESET1_LOW                     | 1.300                  | 1.300                  | 1.310                  |

*Table 6 – Final C2 optimisations for initial test chips*

| <b>B2 Radiation Hardness</b> |       |
|------------------------------|-------|
| <b>TIMINGS (μs)</b>          |       |
| SAMPLE_S                     | 3     |
| SAMPLE_R                     | 3     |
| RESET                        | 14    |
| TX1                          | 8     |
| <b>VOLTAGES (V)</b>          |       |
| VLOADBIAS                    | 2.175 |
| VBIAS1                       | 1.850 |
| VCOLBIAS                     | 2.360 |
| VFLUSH_LOW                   | 1.380 |
| VRESET1_LOW                  | 1.310 |

*Table 7 – Final B2 optimisations for radiation hardness test chips*

APPENDIX C: Per Pixel Analysis Screenshots

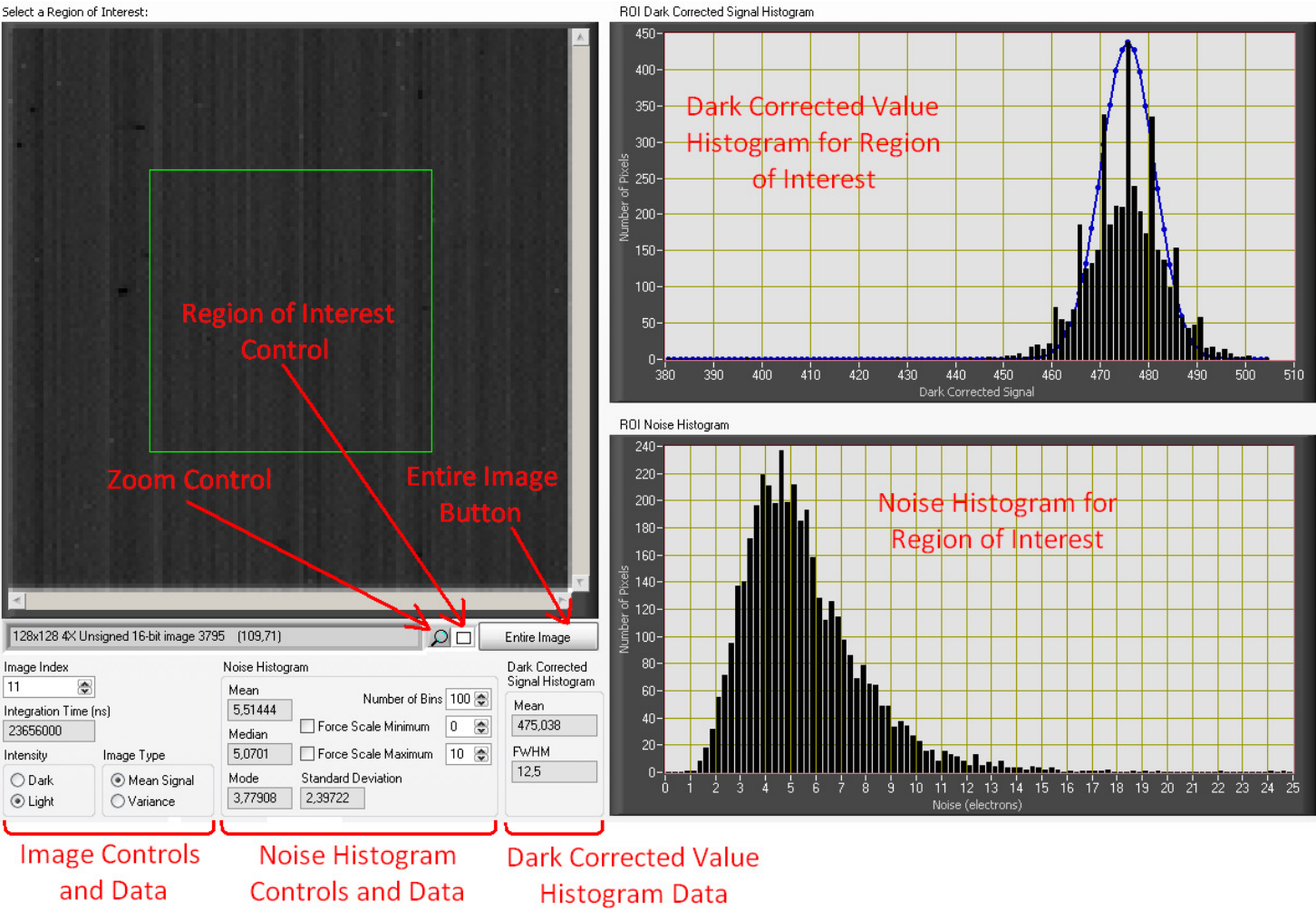
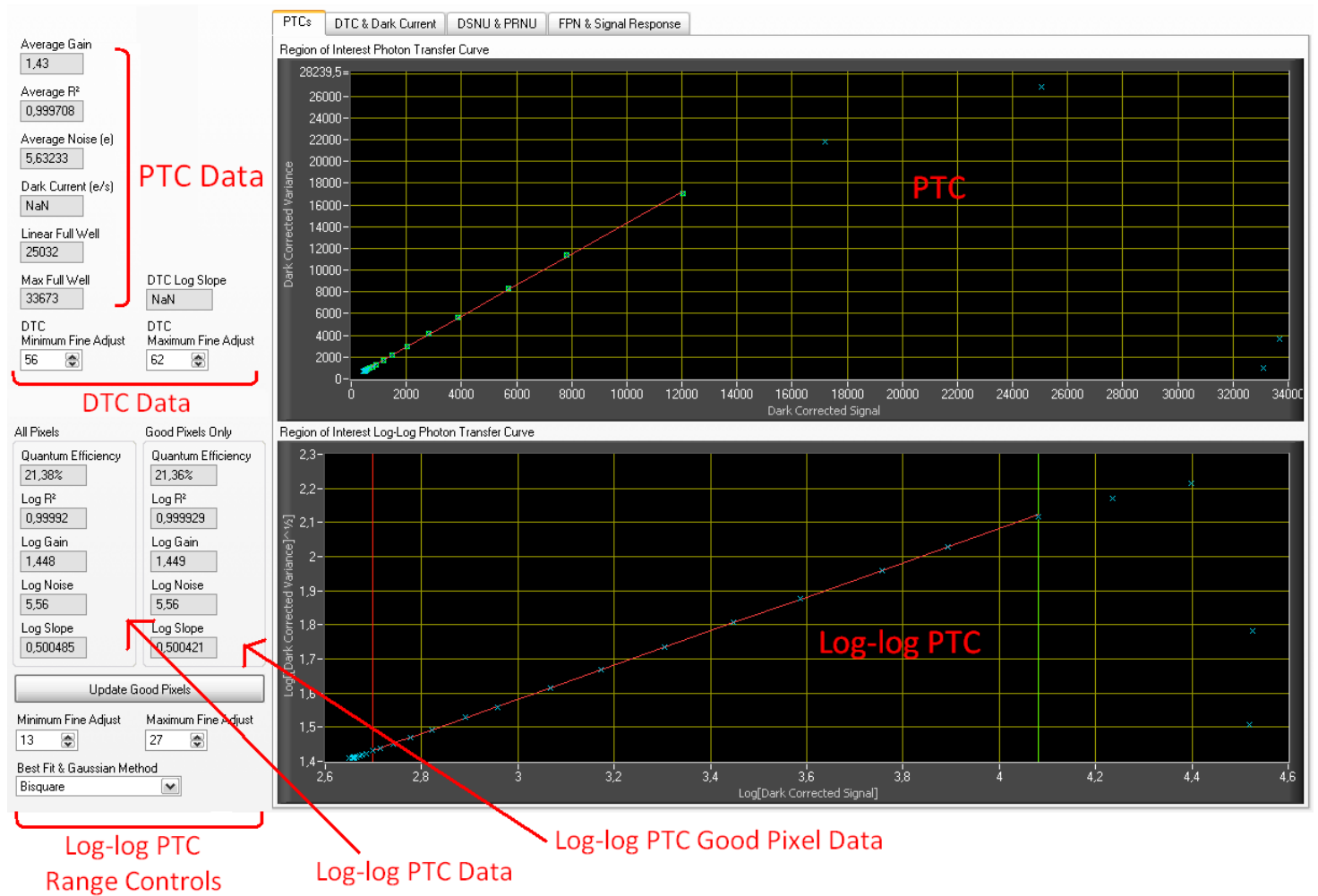
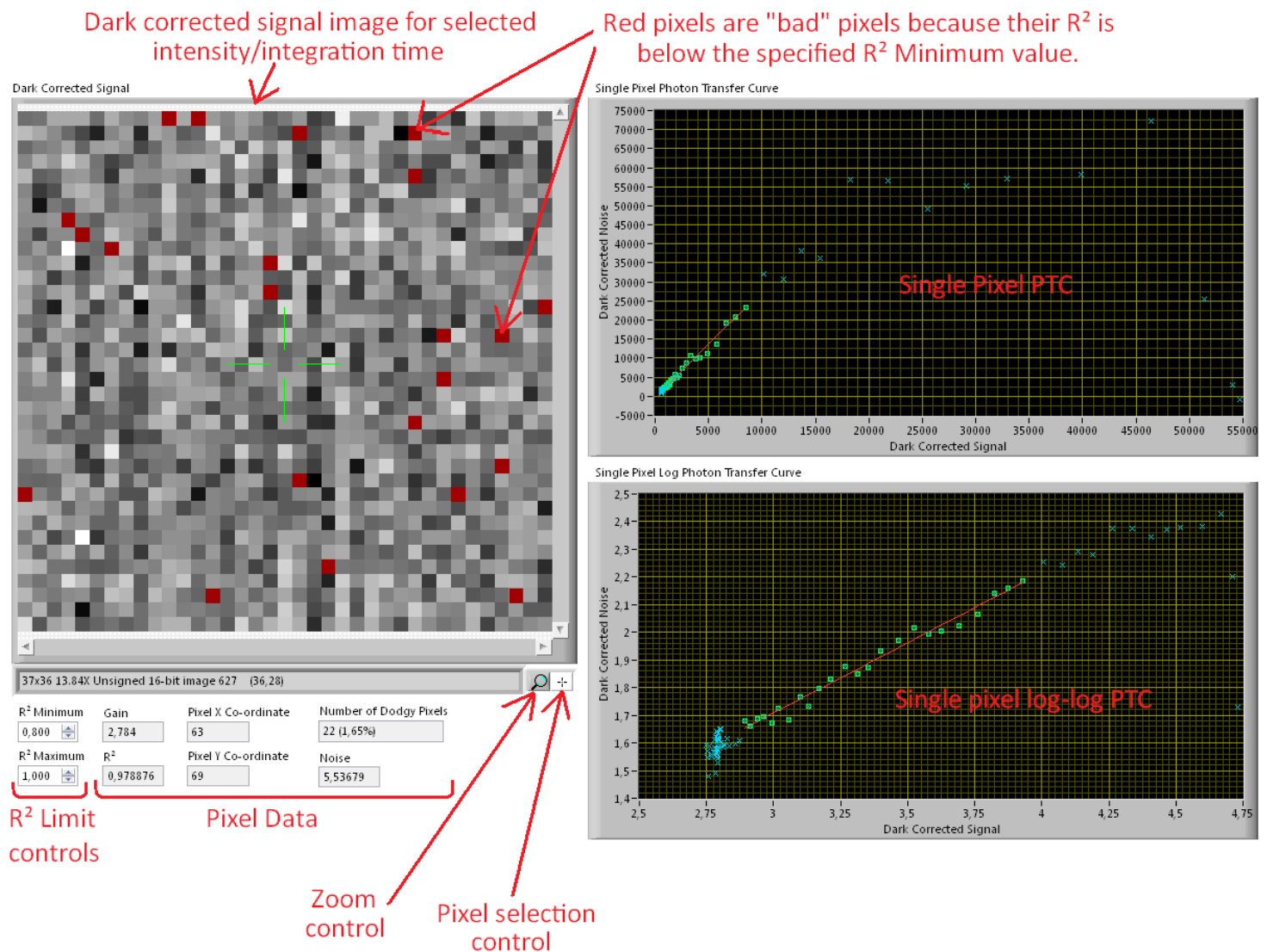


Fig. 60 – Per Pixel Analysis showing the selection of the ROI and histograms of dark corrected signal and noise



**Fig. 61** – Per Pixel Analysis showing the average PTC and log-log PTC of the region of interest, as well as gain and noise calculated from the log-log PTC



**Fig. 62** – Per Pixel Analysis showing highlighted “bad” pixels, a PTC and log-log PTC for a single pixel



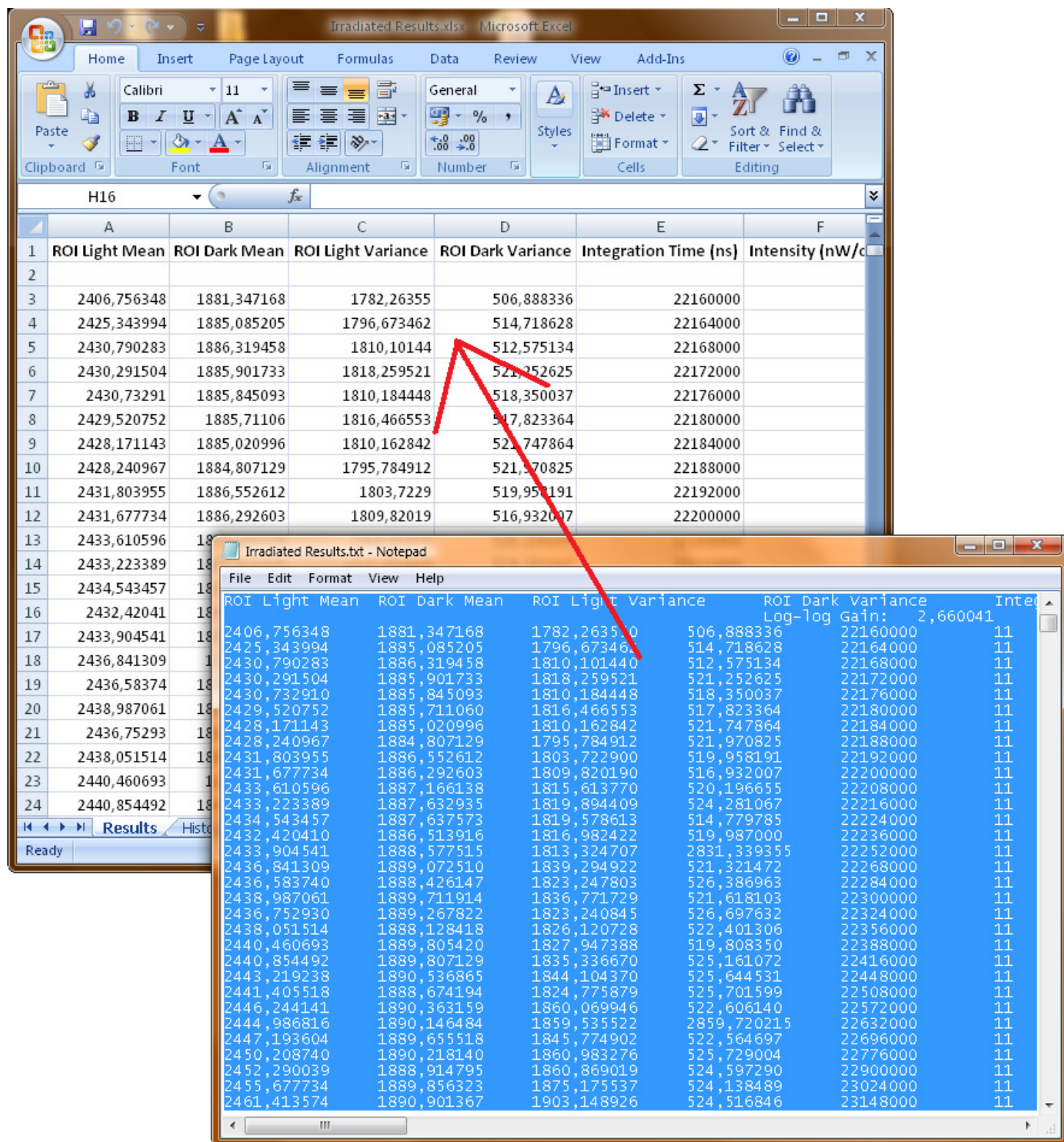
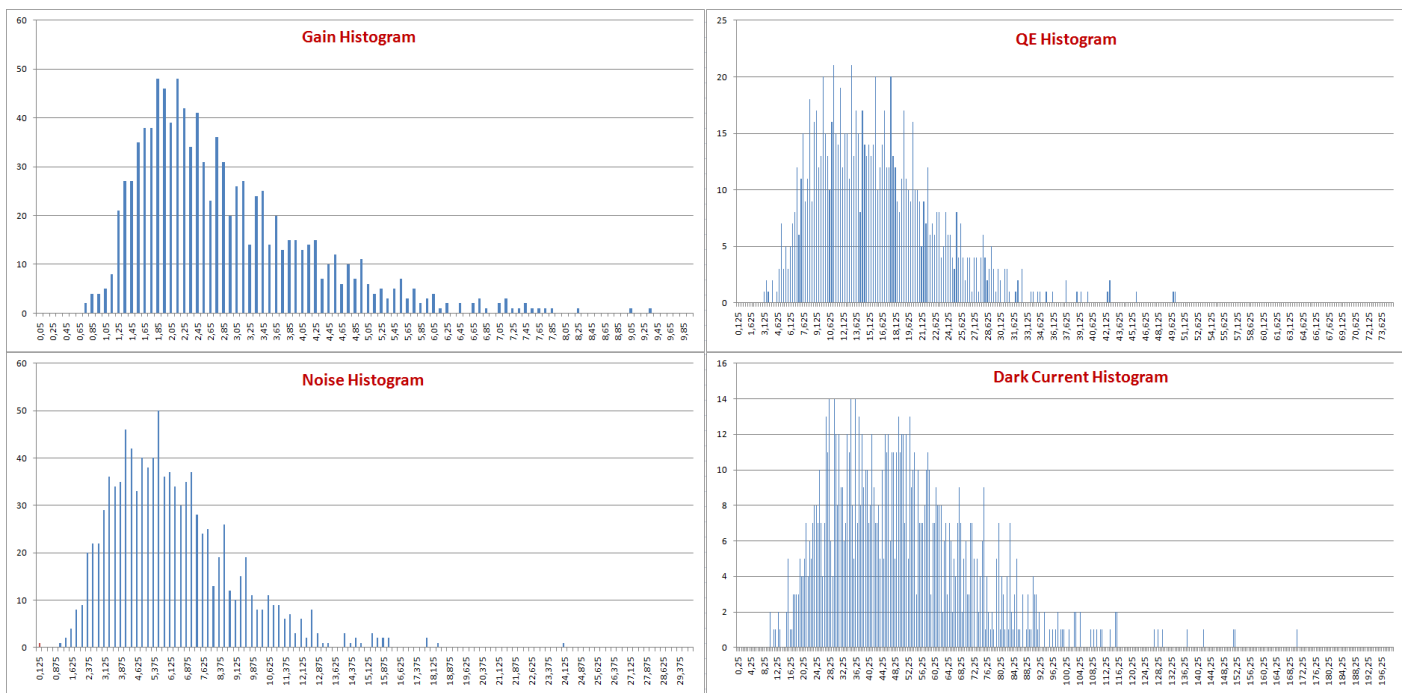
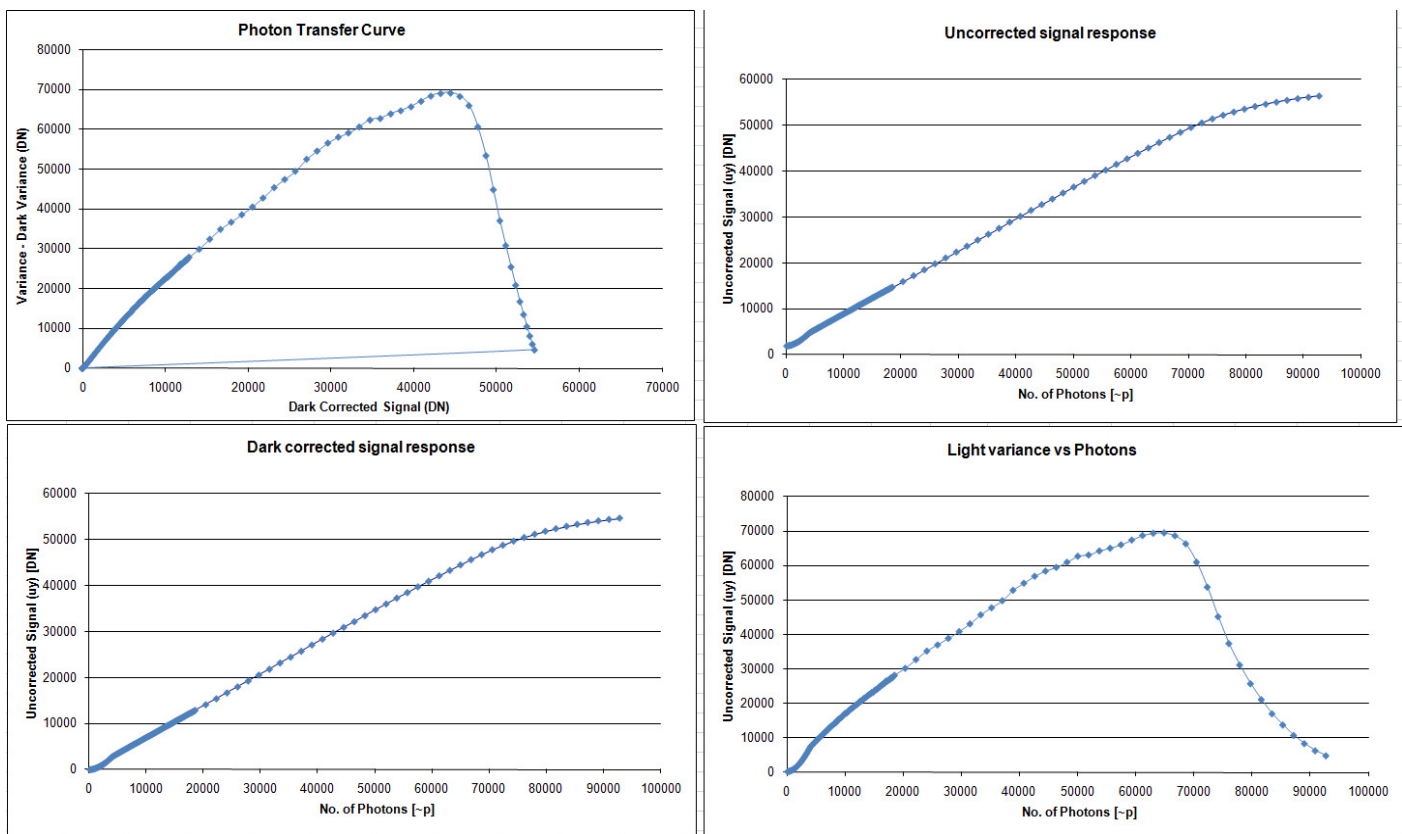


Fig. 63 – Per Pixel Analysis outputted data file and template spreadsheet to generate graphs



**Fig. 64** – Per Pixel Analysis results spreadsheet showing four example histograms for noise, gain, QE and dark current



**Fig. 65** – Per Pixel Analysis results spreadsheet showing four example graphs for PTC, signal response and light variance vs photons